FINAL PROGRAM

SASIMI 2003

The Eleventh Workshop on Synthesis And System Integration of Mixed Information technologies

April 3–4, 2003
International Conference Center Hiroshima, Hiroshima, Japan
http://www.arch.ce.hiroshima-cu.ac.jp/sasimi/

In cooperation with IEEE Hiroshima Section, IEICE, IPSJ, and STARC

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The Eleventh Workshop on Synthesis And System Integration of Mixed Information technologies (SASIMI 2003) will be held at Hiroshima during April 3–4, 2003. Since this workshop started in 1989, SASIMI has provided the researchers and the practitioners who are interested in system design methodology and CAD/DA technologies, with opportunities for interchanging new ideas and for obtaining up-to-date information on the related topics. Many researchers from Asia, U.S.A., and Europe have supported this workshop to make SASIMI one of the major events in this research area. Researchers in the field of system design, VLSI design, VLSI CAD, and VLSI technologies are invited to participate in the workshop.

Program Highlights

Keynote Speech

"Designing Nano-scale Systems for the Ambient Intelligence World,"

Hugo De Man (Katholieke Univ. Leuven/IMEC, Belgium)

Six Invited Talks

- "The Future of IC Design: A Design Technology Point of View," *Raul Camposano (Synopsys, USA)*
- "Advanced Design for Analog-RF and Digital Mixed LSIs –Crosstalk Noise Evaluation and Reduction–,"
  Atsushi Iwata (Hiroshima Univ., Japan)
- "Application-Specific Networks-on-Chips," *Wayne Wolf (Princeton Univ., USA)*
- "Future of Integrated Circuits Technology for the Internet Era," *Yoshio Nishi (Stanford Univ., USA)*
- "Wire Planning for Timing Closure," *Ralph Otten (Technical Univ. Eindhoven, Netherlands)*
- "The MARCO Focus Research Center for Circuits Systems and Software (C2S2): Life at the End of Technology Scaling," *Rob A. Rutenbar (Carnegie Mellon Univ., USA)*

Panel Discussion

"Everything Is (Re-) Programmable And (Re-)Configurable: How Much "Hardware" Is Still Needed?"

Organizer & Moderater

Wolfgang Rosenstiel (Univ. of Tuebingen, Germany)

Panelists

Raul Camposano (Synopsys, USA)
Hugo De Man (Katholieke Univ. Leuven/IMEC, Belgium)
Akira Matsuzawa (Tokyo Inst. of Tech., Japan)
Rob A. Rutenbar (Carnegie Mellon Univ., USA)

Regular Poster Sessions

The format for the meeting is designed to maximize interaction and informal interchange. While full papers are to be published for all contributors, a majority of the presentations are of a poster-board format. That is, each author gives a very short introduction followed by an extended period for informal one-to-one discussions. 50 papers are presented in four sessions:

- System Level Design
- Synthesis, Verification and Testing
- Physical Design
- Design Methodology and Design Experiences

Site of the Workshop

Hiroshima lies in the southwest of Japan's main island. The center of the city is situated in a delta with six rivers, surrounded by mountains and sea. In spring, riverside area, including the convention center and Hiroshima Castle, is colored with beautiful cherry blossoms. In 1996, the A-bomb Dome and Itsukushima Shrine are registered on the UNESCO's World Heritage List.

April 3, Thursday, 2003

9:15-9:30 Opening

9:30-10:45 Keynote Speech (Himawari)

"Designing Nano-scale Systems for the Ambient Intelligence World," *Hugo J. De Man (Katholieke Univ. Leuven/IMEC, Belgium)*

Chair: Shuji Tsukiyama (Chuo Univ., Japan)

10:45-11:00 Break

11:00-11:45 Invited talk 1 (Himawari)

"The Future of IC Design: A Design Technology Point of View," *Raul Camposano (Synopsys, USA)*

Chair: Masahiro Fujita (Univ. of Tokyo, Japan)

11:45-13:15 Lunch Break

13:15-14:00 Invited talk 2 (Himawari)

"Advanced Design for Analog-RF and Digital Mixed LSIs –Crosstalk Noise Evaluation and Reduction–," *Atsushi Iwata (Hiroshima Univ., Japan)*

Chair: Hidetoshi Onodera (Kyoto Univ., Japan)

14:00-15:30 Poster Session 1 (Oral in Himawari, Discussion in Dahlia)

"Logic Level Design/Physical Design I"

Co-Chairs: Hiro Tsujikawa (Matsushita Elec. Ind., Japan)
Yutaka Tamiya (Fujitsu Lab., Japan)

1-1 "A Logic-Synthesis-Friendly RTL Description Style in the SpecC Language," *Y. Sakai(Toshiba Corp., Japan), M. Fujita(Univ. of Tokyo, Japan)*

1-2 "A Design-for-Verification Technique for Reducing Debugging Efforts in HDL," *C. J. Liu(National Central Univ., Taiwan)*

1-3 "Assertion Monitor Based Verification Methodology for Hardware Verification," *S. M. B, M. P, A. S. T. B(International Inst. of Information Technology,Hyderabad, India), K. K. D(Mentor Graphics (India) Ltd, India)*

1-4 "A Layout Design Approach for Low Power Circuits Using On-the-fly Generation of Pass Transistor Logic Cells Based on BDD Structure," *K. Fukuoka, M. Numa, K. Yamamoto(Kobe Univ., Japan), H. Kondoh(Kawasaki Microelectronics, Inc., Japan)*

1-5 "A Hybrid Approach Combining Symbolic and Structural Techniques for Disjoint SOP Minimization," *G. Fey, R. Drechsler(Univ. of Bremen, Germany)*

1-6 "An Improved Multiple Error Diagnosis Technique Using Symbolic Simulation with Truth Variables and Its Application to Incremental Synthesis for Standard-Cell Design," *H. Inoue, T. Iwasaki, M. Numa, K. Yamamoto(Kobe Univ., Japan)*

1-7 "Statistical Gate-delay Modeling with Intra-gate Variability," *K. Okada, K. Yamaoka, H. Onodera(Kyoto Univ., Japan)*

1-8 "Extraction of Inter- and Intra-Chip Device-Parameter Variations with a Differential-Amplifier-Stage Test Circuit," *T. Mizoguchi, H. J. Mattausch, H. Ueno, D. Kitamaru, K. Hisamitsu, M. Miura-Mattausch(Hiroshima-university, Japan), S. Itoh, K. Morikawa(STARC, Japan)*

1-9 "Efficient Techniques for Reducing Substrate Model Complexity in Mixed-Signal IC's," *H. Lan, Y. Lu(Stanford Univ., USA), N. Nakano(Keio Univ., Japan), R. W. Dutton(Stanford Univ., USA)*

1-10 "Rectangle-based Layout Conversion for Migration," *Y. Choi, I. Chun, B. Kim(Chungnam National Univ., Korea)*

1-11 "Cell Placement Optimization Using Phase Transition and Annealing by a Metropolis's Monte-Carlo Simulation," *M. Toyonaga(Kochi Univ., Japan), K. Kurokawa(Matsushita Elec. Ind. Co.,Ltd., Japan), T. Akino(Kinki Univ., Japan), S. Kuninobu(Kochi Univ., Japan)*

1-12 "Design Optimization Methodology of On-Chip Spiral Inductor," *H. Hoshino, K. Okada, H. Onodera(Kyoto Univ., Japan)*

15:30-16:15 Invited talk 3 (Himawari)

"Application-Specific Networks-on-Chips," *Wayne Wolf (Princeton Univ., USA)*

Chair: Kazutoshi Wakabayashi (NEC, Japan)

16:15-17:45 Poster Session 2 (Oral in Himawari, Discussion in Dahlia)

"System Level Design/Design Experiences I"

Co-Chairs: Yukihiro Iguchi (Meiji Univ., Japan)
Nozomu Togawa (Univ. of Kitakyushu, Japan)

2-1 "A Front-end for Better Handling of High-level Hardware Descriptions," *L. Gauthier(IST, Japan), N. Devroye, H. Tomiyama, K. Murakami(ISIT, Japan)*

2-2 "Bit Length Optimization of Fractional Parts on Floating to Fixed Point Conversion for High-Level Synthesis," *N. Doi(NAIST, Japan), T. Horiyama(Kyoto Univ., Japan), M. Nakanishi(NAIST, Japan), S. Kimura(Waseda Univ., Japan), K. Watanabe(NAIST, Japan)*

2-3 "A Voltage Scheduling Technique for Fault-Tolerant Real-Time Microprocessor Systems," *T. Ishihara(Univ. of Tokyo, Japan)*

2-4 "Binding Constrained Scheduling for Iterative Algorithm with Conditional Branches," *K. Ohashi, M. Kaneko(JAIST, Japan)*

2-5 "A Simulator Generator Based on Configurable VLIW Model Considering Synthesizable HW Description and SW Tools Generation," *K. Okuda, S. Kobayashi, Y. Takeuchi, M. Imai(Osaka Univ., Japan)*

2-6 "An Instruction-Set Simulator Generator for SIMD Processor Cores," *Y. Miyaoka(Waseda Univ., Japan), N. Togawa(The Univ. of Kitakyushu, Japan), K. Kasahara, J. Choi, M. Yanagisawa, T. Ohtsuki(Waseda Univ., Japan)*

2-7 "A Prioritized Cache for Multi-tasking Real-Time Systems," *Y. Tan, V. J. Mooney III(Georgia Inst. of Tech., USA)*

2-8 "Hardware Implementation of Binary Morphological Operations Based on Decomposition of Structure Element," *K. Thammajong(King Mongkut's Univ. of Tech. Thonburi, other), K. Chamnognthai(The Univ. of the Thai Chamber of Commerce, other), P. Kumhom(King Mongkut's Univ. of Tech. Thonburi, other)*

2-9 "Architectural Design Space Exploration of Configurable Processors Using ASIP Meister," *A. Kitajima(Osaka Electro-Communication Univ., Japan), Y. Takeuchi(Osaka Univ., Japan), A. Shiomi(Shizuoka Univ., Japan), J. Sato(Tsuruoka National College of Tech., Japan), S. Kobayashi, M. Imai(Osaka Univ., Japan)*

2-10 "Design and Analysis of Hardware Acceleration for Ethernet TCP/IP Checksum Computation," *I. Huang, R. Gu, Z. Chen(National Sun Yat-Sen Univ., Taiwan)*

2-11 "Development of an IP Library of IEEE-754-Standard Single-Precision Floating-Point Dividers," *H. Ochi, T. Suzuki, S. Matsunaga, Y. Kawano, T. Tsuda(Hiroshima City Univ., Japan)*

2-12 "An Associative Memory for Real-Time Applications Requiring Fully Parallel Nearest Manhattan-Distance-Search," *T. Koide, Y. Yano, H. J. Mattausch(Hiroshima Univ., Japan)*

2-13 "A Design of Neural Signal Sensing LSI with Multi-Input-Channels," *T. Yoshida, T. Mashimo, M. Akagi, A. Iwata, M. Yoshida, K. Uematsu(Hiroshima Univ., Japan)*

18:30-20:30 Banquet (ANA Hotel)

April 4, Friday, 2003

9:00-9:45 Invited talk 4 (Himawari)

"Future of Integrated Circuits Technology for the Internet Era," *Yoshio Nishi (Stanford Univ., USA)*

Chair: Takashi Kambe (Kinki Univ., Japan)

9:45-11:15 Poster Session 3 (Oral in Himawari, Discussion in Dahlia)

"Logic Level Design/Physical Design II"

Co-Chairs: Masanori Hashimoto (Kyoto Univ., Japan)
Yasuhiro Takashima (JAIST, Japan)

3-1 "An Approach for Circuit Size Reduction by Variable Reordering for PCA-Chip2," *T. Yuasa, A. Tomita, T. Izumi(Kyoto, Japan), T. Onoye(Osaka, Japan), Y. Nakamura(Kyoto, Japan)*

3-2 "A Method to Realize Logic Functions Using LUTs and OR Gates," *M. Matsuura, T. Sasao(Kyushu Inst. of Tech., Japan)*

3-3 "Dynamic Effective Precision Matching Computation," *V. Goulart, K. Murakami(Kyushu Univ., Japan)*

3-4 "VHDL Modeling of MPEG Audio Decoder," *M. B. I. Reaz, M. S. Sulaiman(Multimedia Univ., Malaysia), M. A. M. Ali(Univ. Kebangsaan Malaysia, Malaysia)*

3-5 "On Strong Locality Properties of Alternative Wires in Digital Circuits," *Y. L. Wu(The Chinese Univ. of Hong Kong, Hong Kong), H. Fan(Univ. of Victoria, Canada), W. Wong, K. C. Cheng, C. C. Cheung(The Chinese Univ. of Hong Kong, Hong Kong)*

3-6 "The Design of Sfl2vl: SFL to Verilog Convertor Based on a LR-parser," *N. Shimizu(Tokai Univ., Japan)*

3-7 "Code Generation for Embedded Systems Using Heterogeneous MDDs," *S. Nagayama, T. Sasao(Kyushu Inst. of Tech., Japan)*

3-8 "Driving Capability by Lateral BJT-CMOS Inverter," *T. Akino(Kinki Univ., Japan)*

3-9 "Timing-Driven Standard Cell Placement with a New Cluster Placement Model," *H. Kubota, N. Iwauchi, S. Wakabayashi(Hiroshima Univ., Japan)*

3-10 "Slew Calculation against Diverse Gate-Input Waveforms for Accurate Static Timing Analysis," *Y. Yamada, M. Hashimoto, H. Onodera(Kyoto Univ., Japan)*

3-11 "Frequency Determination for Interconnect RLC Extraction," *A. Tsuchiya, M. Hashimoto, H. Onodera(Kyoto Univ., Japan)*

3-12 "A Parasitic Capacitance Modeling Method for Non-Planar Interconnects," *S. Tani, Y. Uchida, M. Furuie(Osaka Univ., Japan), S. Tsukiyama(Chuo Univ., Japan), B. Lee, S. Nishi, Y. Kubota(SHARP Corp., Japan), I. Shirakawa(Osaka Univ., Japan), S. Imai(SHARP Corp., Japan)*

11:15-12:00 Invited talk 5 (Himawari)

"Wire Planning for Timing Closure," *Ralph Otten (Technical Univ. Eindhoven, Netherlands)*

Chair: Youn-Long Lin (Tsing Hua University, Taiwan)

12:00-13:30 Lunch Break

13:30-14:15 Invited talk 6 (Himawari)

"The MARCO Focus Research Center for Circuits Systems and Software (C2S2): Life at the End of Technology Scaling," *Rob A. Rutenbar (Carnegie Mellon Univ., USA)*

Chair: Tetsuya Fujimoto (STARC, Japan)

14:15-15:45 Poster Session 4 (Oral in Himawari, Discussion in Dahlia)

"System Level Design/Design Experiences II"

Co-Chairs: Tomonori Izumi (Kyoto Univ., Japan)
Hiroshi Date (System JD, Japan)

4-1 "Verification Environment for C-Based Design," *H. Makida, T. Morishita, M. Ohnishi, K. Okada, A. Yamada, T. Kambe(Sharp Corp., Japan), P. Boca(Sharp Laboratories of Europe Limited, UK)*

4-2 "Optimized Bank-Based Multi-Port Memories through a Hierarchical Multi-Bank Structure," *S. Fukae, N. Omori, H. J. Mattausch, T. Koide(Hiroshima Univ., Japan), T. Inoue, T. Hironaka(Hiroshima City Univ., Japan)*

4-3 "Behavioral Simulation Techniques for Substrate Noise Analysis in PLL Circuits," *J. W. Kim(Stanford Univ., USA), M. H. Perrott(M.I.T., USA), R. W. Dutton(Stanford Univ., USA)*

4-4 "High-level Control Flow Transformations for Performance Improvement of Address-Dominated Multimedia Applications," *H. Falk(Univ. of Dortmund, Germany), C. Ghez, M. Miranda(IMEC Lab., Belgium), R. Leupers(RWTH Aachen Univ., Germany)*

4-5 "An Efficient Power and Performance Evaluation Method with Reconfigurable Bus Architecture Model," *M. Takahashi, H. Miyajima, M. Fukui(Matsushita, Japan)*

4-6 "Heterogeneous Processor Architecture and Its Design Methodology to Shorten the Design Period of Embedded SoCs," *Y. Yuyama, M. Aramoto, K. Takai(Kyoto Univ., Japan), K. Kobayashi(Tokyo Univ., Japan), H. Onodera(Kyoto Univ., Japan)*

4-7 "DX-Gt: Memory Management and Crossbar Switch Generator for Multiprocessor System-on-a-Chip," *M. A. Shalan, E. S. Shin, V. J. Mooney III(Georgia Tech, USA)*

4-8 "VLSI Architecture for MPEG-4 Core Profile Codec Core," *T. Nakagawa, G. Fujita, T. Onoye, I. Shirakawa(Osaka Univ., Japan)*

4-9 "Scalable Design Framework for JPEG2000 Encoder Architecture," *Y. Hayashi, H. Tsutsui, T. Masuzaki, T. Izumi, T. Onoye, Y. Nakamura(Kyoto Univ., Japan)*

4-10 "Implementing Image Processing Algorithms on FPGA-based Realtime Vision System," *S. Hirai, M. Zakouji, T. Tsuboi(Ritsumeikan Univ., Japan)*

4-11 "Taking Over Mechanism: a Cooperation Methodology of Hardware and Software in Network Controllers," *K. Watanabe, H. Amano(Keio Univ., Japan), J. Yamamoto(Hitachi, Ltd. Central Research Laboratory, Japan), J. Tsuchiya, T. Otsuka(Keio Univ., Japan), T. Kudoh(National Inst. of Advanced Industrial Science and Tech., Japan)*

4-12 "High Access Bandwidth Multi-Port-Cache Design with Compact Hierarchical 1-Port-Bank Structure," *Z. Zhu, K. Johguchi(Hiroshima Univ., Japan), T. Hirakawa(Hiroshima City Univ., Japan), H. J. Mattausch, T. Koide(Hiroshima Univ., Japan), T. Hironaka(Hiroshima City Univ., Japan)*

4-13 "A Novel Wide Operating Range Technique of Delay-Locked Loop with Frequency Selection Block," *W. Chang, C. Lien, T. He(Tamkang Univ., Taiwan)*

15:45-17:15 Panel discussion (Himawari)

"Everything Is (Re-) Programmable and (Re-) Configurable: How Much "Hardware" Is Still Needed?"

Organizer & Moderator

Wolfgang Rosenstiel (Univ. of Tuebingen, Germany)

Panelists:

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17:15-17:30 Closing

SASIMI 2003 CDROM Proceedings are available!

The price of each CDROM is 3,000 Japanese Yen. Please fill the order form and come to the reception desk.