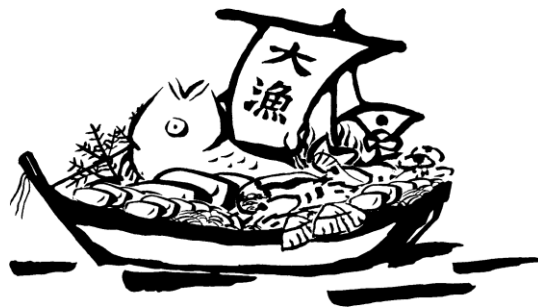# Call for Participation

SASIMI 2013

THE 18TH WORKSHOP ON
SYNTHESIS AND SYSTEM INTEGRATION
OF MIXED INFORMATION TECHNOLOGIES

October 21–22, 2013
Hotel Sapporo Garden Palace, Sapporo, Japan

In cooperation with: Institute of Electrical and Electronics Engineers (IEEE), Sapporo Section
IEEE Circuits and Systems Society, Japan Chapter
The Institute of Electronics, Information and Communication Engineers (IEICE)
Information Processing Society of Japan (IPSJ)
Supported by: Semiconductor Technology Academic Research Center (STARC)
The Telecommunications Advancement Foundation

Aims of the Workshop

This workshop provides an interchange forum on system design, design experiences, EDA, and design methodologies for both of industry and academy. Many researchers of Asia, U.S. and European countries in the area of hardware design methodology have supported this workshop and made SASIMI one of the most famous events in this research area. The workshop gives a good opportunity for discussion on advanced work and research. Researchers in the field of system design, VLSI design, VLSI CAD, and VLSI technologies are welcome to this workshop.

Keynote Speeches

- Nikil Dutt (UC Irvine) , "Scaling the Many-Memory Wall for Many-Core Architectures"
- Rudy Lauwereins (IMEC) , "Replacing Optical Lenses by Silicon Structures"

Invited Talks

- Naehyuck Chang (Seoul National Univ.),
  "Computer-aided Design of Electric Vehicle Hybrid Energy Storage System"
- Shin-ichi Minato (Hokkaido Univ. / JST) ,
  "Power of Enumeration --- State-of-the-art Algorithms for Tackling Combinatorial Explosion"
- Tsung-Yi Ho (National Cheng Kung Univ.) , "Physical Design of Microfluidic Biochips"

Panel Discussion

"Application of EDA Technologies to Non-EDA Areas"
- Organizer/Moderator: Masahiro Fujita (Univ. of Tokyo)
- Panelists: Rudy Lauwereins (IMEC), Shin-ichi Minato (Hokkaido Univ. / JST),
  Tsung-Yi Ho (National Cheng Kung Univ.), Giovanni De Micheli (EPFL), Kazutoshi Wakabayashi (NEC)

Regular Poster Sessions

This workshop is designed to maximize interaction and informal interchange. While full or short papers are to be published for all contributors, a majority of the presentations are of a poster-board format. That is, each author gives a very short introduction followed by an extended period for informal one-to-one discussions. Many "fresh" papers are to be presented in regular poster sessions on the topics including System Level Design, Logic Design, Physical Design, and Design Experiences.
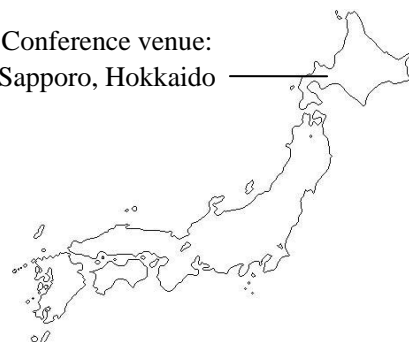
Registration

All the participants, including keynote/invited speakers, panelists, moderators, and session chairs, are required to make registration.
The deadline for advance registration (via WWW) is September 20, 2013.

Conference venue:
Sapporo, Hokkaido

Questions should be directed to:

SASIMI 2013, c/o Prof. Nagisa Ishiura

School of Science and Technology, Kwansei Gakuin University
2-1 Gakuen, Sanda, Hyogo 669-1337, Japan

E-mail: sasimi13@sasimi.jp

For More and Latest Information: `http://sasimi.jp/`