A Hardware Generator for Aesthetic Nonlinear Filter Banks

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Abstract— This paper considers hardware realizations of nonlinear filter banks for facial beautification. First, users describe filters' characteristics and how to connect them using filter bank description languages (FDLs), then the proposed system generates Verilog HDLs to realize them. Preliminary experimental results show that generated HDLs have the same performance as ones coded by hands.

I. Nonlinear Filter Banks for Face Image Beautification

Nonlinear filter banks were proposed before for the face image beautification, being named as aesthetic filter banks[2]. Figure. 1 shows the structure of the aesthetic filter bank, which includes a linear filter and three nonlinear filters named ϵ-filters. ϵ-filters can effectively reduce small-amplitude and high-frequency noise embedded in large-amplitude signals[1].

The input-output relation of the ϵ-filters is represented as (1), where $x(n)$ and $y(n)$ are the input and output signals at time n respectively. a_i's are coefficients of a non-recursive low-pass filter such that (2). F is a nonlinear function as shown in fig. 2.

$$y(n) = x(n) + \sum_{i=-N}^{N} a_i F(x(n+i) - x(n)), \quad (1)$$

$$\sum_{i=-N}^{N} a_i = 1. \quad (2)$$

Aesthetic filters can separate input signals into five regions as shown in fig. 3. Human faces are disfigured by spots ($y_3(n)$) and wrinkles ($y_4(n)$). Face structures ($y_1(n)$ and $y_2(n)$) and natural roughness ($y_5(n)$) are necessary for faces. We can beautify human faces by extracting $y_1(n)$, $y_2(n)$, and $y_5(n)$, and summing them up.

We can realize aesthetic filters for embedded devices by using embedded MPUs or digital signal processors (DSPs). However, jumpy/frame rate problems may occur when the size of window in each filter is large. We would also like to reduce the power consumption.

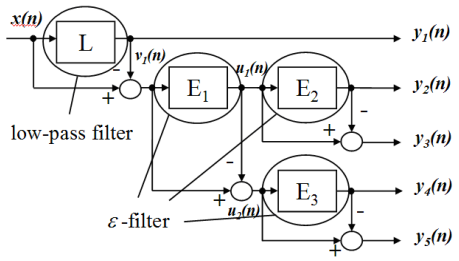

Fig. 1. Structure of aesthetic filter bank.

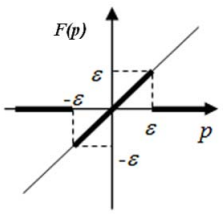

Fig. 2. Example of nonlinear function F.

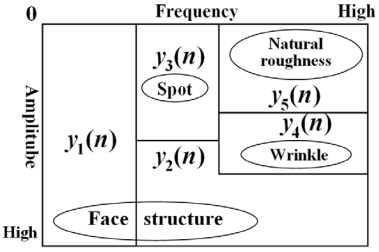

Fig. 3. Five regions for human faces separated by aesthetic filters.

One solution is to realize dedicated hardwares for aesthetic filters. Since the face image beautification includes subjective elements, we often change parameters and/or structures of filter banks. However, redesigning aesthetic filters should increase costs. We have developed a synthesis system for filter banks.

II. Hardware Generator for Aesthetic Filters

From here we describe FDL2V, a hardware generator for filter banks. We have developed FDL2V in Perl with 3,379 source lines of codes. First, users can describe structures of filter banks and their parameters by using FDLs (filter bank description languages)[3]. Then the system generates Verilog HDLs (hardware description languages) for dedicated filter banks. Figure 5(b) shows FDL2V. It includes a lexical analyzer, a syntactic analyzer, and a code generator. Figure 5(a) shows an example of FDL codes which describes the aesthetic filter shown in fig. 1. FDL2V computes depths of buffered, synchronous pipelines and inserts them in the verilog HDL codes automatically. Figure 7 shows the block diagram synthesized by the FPGA development system from the verilog HDL code generated by FDL2V. Figure 6 shows the one of the ϵ-filters in fig. 4, where the window size is 5×5.

III. Experimental Results and Comments

To evaluate performance of the generator FDL2V, we implemented aesthetic filters generated by FDL2V and ones codes by hand on the FPGA education board Terasic DE2-115. Altera Cyclone IV EP4CE115F29C7N device is equipped on it. We used Altera Quartus II ver. 13.0 for

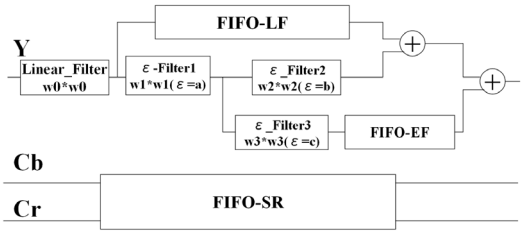

Fig. 4. Filter bank circuit generated by FDL2V.

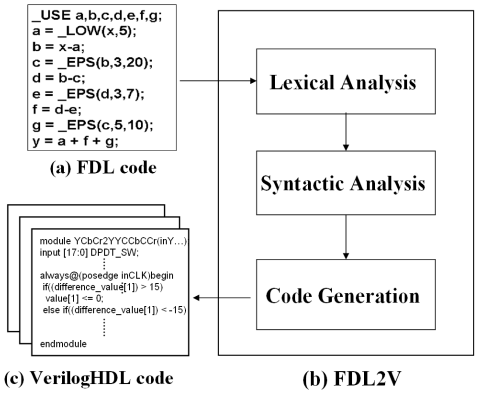

Fig. 5. Hardware generator: FDL2V.

developing. We checked that they were working without problems.

Figure. 7 explains how to process facial images on the DE2-115 board. A CCD camera is connected to the TV-in connector, and NTSC signals are converted into YCbCr ones, where Y is the luminance component and Cb and Cr are the blue-difference and red-difference chroma components. While aesthetic filters processes only Y signals by the ϵ-filter bank, Cb and Cr signals are delayed by FIFOs. YCbCr signals are converted to RGB ones, Finally, we can get beautified facial images.

FDL2V can not only generate Verilog HDL codes for aesthetic filters but also other functions to handle NTSC

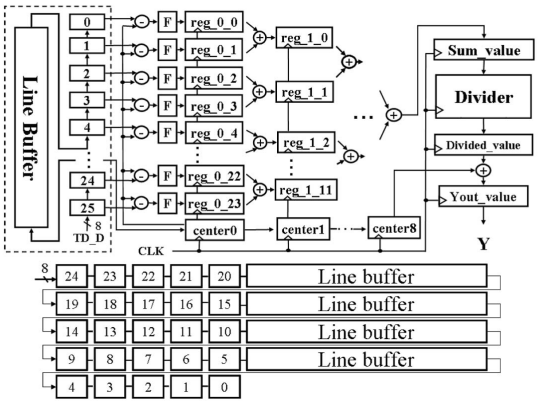

Fig. 6. ϵ-filter generated by FDL2V.

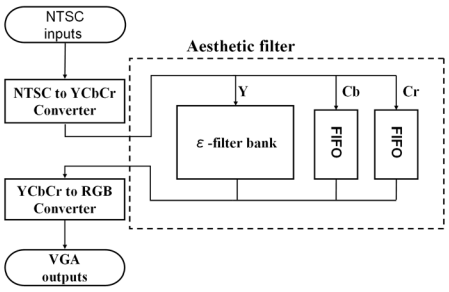

Fig. 7. Aesthetic filter on DE2-115.

TABLE I
SYNTHESIS RESULT

	FDL2V	Hand coding	Max size
#LEs	4,808 (4%)	4,329 (4%)	114,480
#M9Ks	42 (10%)	43 (10%)	432
Mem [bits]	315,492 (8%)	302,217 (8%)	3,981,312
HDL SLOC	2,065	1,988	-
FDL SLOC	9	-	-
Power [mW]	304.3	270.4	-

Clock rate: 50 [MHz], Altera Cyclone IV EP4CE115F29C7N.

and YCbCr signals by using devices on the DE2-115.

Table I shows the preliminary experimental results. The FPGA has 114,480 Logic Elements and 432 M9Ks (embedded memories). Maximum memory size is 3,981,312 [bits]. We developed two aesthetic filters from Verilog HDL codes generated by FDL2V and coded by hands, where the resolution is 640×480 and window sizes of L, E_1, E_2, and E_3 are 5×5, 3×3, 5×5, and 3×3 respectively.

Two results use almost same usage rate of resources, LEs, M9Ks, and Mem. Source lines of codes (SLOC) of them are 2,065 and 1,988. Please note that FDL2V users only have to write 9 SLOC by the FDL, and then FDL2V generates Verilog HDL codes in 12 [sec] with a Core i7, 2.8 GHz PC. One by FDL2V requires 13% larger power consumption than one for the hand coding. The reason is that registers' length coded by hand are optimized.

We have developed a hardware generator for real time aesthetic filters. Users can dramatically reduce coding hours, and test and evaluate aesthetic filters for various window sizes, values of ϵ, image sizes.

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