Low-power Op-amp with Capacitor-base On-chip Power Supply

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Abstract— This paper presents a low-power analog system with a mechanism which provides a power supply via rechargeable capacitor. The system is promising for sensor systems with energy harvesting mechanism. We implement a capacitor-base power supply using MIM structure, and provide a case study which a nano-watt op-amp operates in the proposed system. The simulation results show that the op-amp works for an hour by 1 μF charge to the capacitor.

I. Introduction

In recent years, sensor systems become to be used in various fields such as an automatic diagnosis to discover abnormality and the damage in the building, the measurement of water, temperature of the soil in the agriculture, and the measurement of a heart rate and breathing in the medical.

In the development of integrated circuits for such sensor systems, long life-time, low power consumption become key technologies. Additionally, an energy harvesting technology for generating electricity using envionmental energy is promising. On the other hand, sensor systems require further downsizing, Therefore, on-chip power supply and electricity generation using MEMs are studied.

This paper presents a power supply mechanism for an analog circuit based on an on-chip capacitor which is applicable to sensor systems. We use an low-power op-amp as an example of analog circuits, and verify the possibility of the proposed system.

First, we introduce the charging mechanism using MIM-type capacitor to the power supply, which is comparatively realizable low cost. From the external of the chip, we charge 1 μF electricity to the MIM-type capacitor, and the electricity is provided to the the op-amp via a virtual power supply wire with a switch.

We design a nano-watt op-amp with a nano-watt CMOS reference circuit which are promising to be used in sensor analog front-end system. In these circuit, several MOSFETs operate in the subthreshold region, and are biased as flowing a circuit nA current. Moreover, both circuits are connected to a virtual power supply wire, and the electricity are supplied only from the MIM-type on-chip capacitor.

In this paper, we implement the charging mechanism and analog circuits on 65nm CMOS process. The simulation result shows that the op-amp works for an hour by one charging of 1 μF.

The rest of this paper is organized as follows; Section 2 describes the MIM-type on-chip capacitor and low-power analog circuits, and Section 3 introduces the proposed system. Section 4 is devoted into describing the characteristic of the op-amp and its specification. Section 5 reports the simulation result of the proposed system, and Section 6 concludes our works.

II. preparation

This section explains the element circuits which constitute a proposed system.

A. MIM-type capacitance

In this work, we adopt the MIM-type implementation as a typical on-chip capacitor. The sectional view of the MIM-type capacitor is shown in Fig. 1. The area density when the MIM-type capacitor in a 65-nm CMOS process is $1.0\mu m^2/fF$. Therefore, realizing capacitor of $1.0\mu F$, we need the area of $10^9\mu m^2$, i.e., the on-chip capacitor of $3.3cm \times 3.3cm$. Although this area looks huge as an on-chip capacitance, the implementation of smaller capacitors will be dealt with as a future subject.

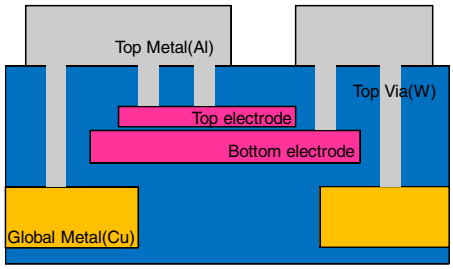

Fig. 1. The sectional view of MIM-type capacitor

B. Low-power Op-amp

In order to drive an analog circuit by the limited electricity charged in the capacitor, it is important that the analog circuit

itself should be as low power as possible. We adopt a nW class op-amp circuit which is proposed in [1].

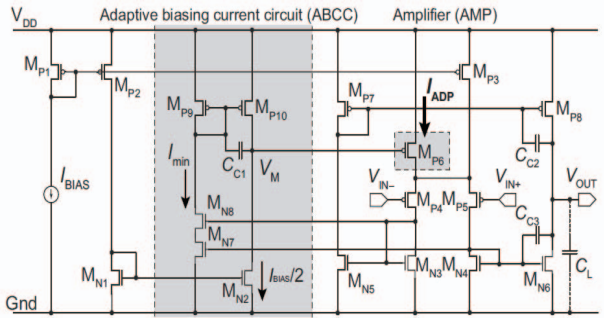

Fig. 2. Op-amp circuit with adaptive biasing

The circuit diagram of the op-amp is shown in Fig. 2, which is composed of a two-stage op-amp circuit and an adaptation bias current generation circuit (ABCC). An ABCC circuit constitutes a feedback loop and it operates depending on input voltage. If $V_{IN-} = V_{IN+}$, V_M is determined such that $I_{ADP} = I_{BIAS}/2$. On the other hand, if $V_{IN-} \neq V_{IN+}$, the value of V_M falls and I_{ADP} is amplified. That is, in $V_{IN-} \neq V_{IN+}$, the amplified I_{ADP} is supplied to an op-amp, and the circuit operates at the high-speed.

C. CMOS Reference Circuit

Next, in order to generate the reference current used in the op-amp, we adopt nA reference circuit introduced in [2]. The circuit diagram of this circuit is shown in Figure 3.

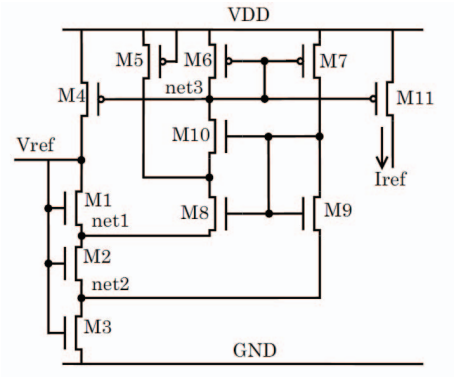

Fig. 3. *nA* reference circuit

M1-M3 in the Figure 3 operate in a subthreshold region, and they yield a nA current. Moreover, M8 serves a temperature compensating circuit such that the leakage current of M9 makes it balance, and M5 operates in a cutoff region. Although [2] proposes as Iref= $2nA$, we redesign the circuit to provide $50nA$.

III. Our Proposed System

In this section, we propose a power supply system with a MIM-type on-chip capacitor for driving analog circuits.

The structure of the proposed system is shown in Figure 4. The system is composed of a capacitor C, a switch block, a virtual power source wire, and an analog circuit (circuit block). First, connecting a switch to a V_{ch} side, we charge the capacitor C. Then, we change the connection of a switch to the virtual power supply wire side to supply the collected electric charge to the circuit block side.

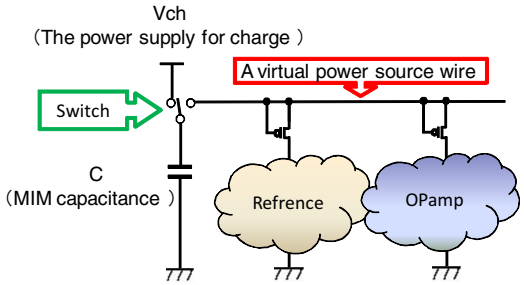

Fig. 4. The structure of our proposed system

Following, a switch block and a circuit block are explained.

A. Switch Block

The circuit diagram of a switch block is shown in Figure 5. It consists of the transfer gates for discharging and the P-MOS switch for charging V_{ch} at the capacitor C. The discharge means that the electric in the capacitor C moves to virtual power supply wire V_{out}. When charging, the input, V_b, of the switch is set to "0" and the input V_{sw} is set to "1". Moreover, when discharging an electric charge to virtual power supply wire V_{out}, the inputs of V_b and V_{sw} are "1" and "0", respectively.

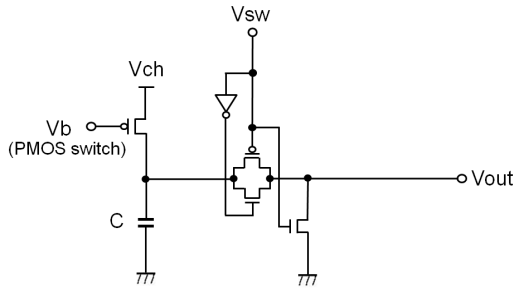

Fig. 5. Switch block

Figure 6 shows the simulation result of the switch operation.

1. In the period (1), it performs a charge to the capacitor C from the external power supply V_{ch}.

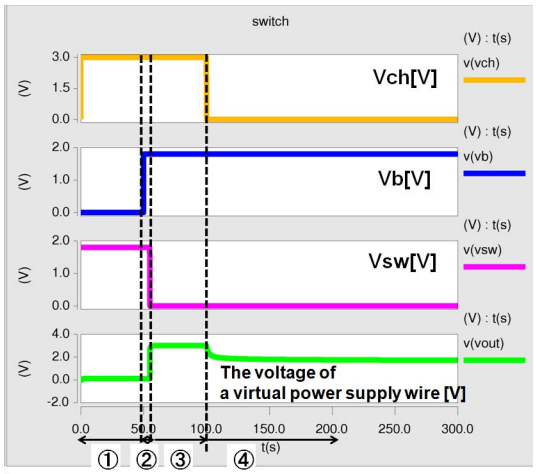

Fig. 6. Virtual power supply wire voltage for parameter settings

2. In the period (2), it disconnects the capacitor C to the external. In details, after charing C, it sets V_b to be "1", disconnects C, and sets V_{sw} to "1" to discharge an electric charge to a virtual power supply wire.

3. In the period (3), it discharges the electric charge in C to the virtual power supply wire side. However, the connection to the external remains to avoid exhausting an electric charge instantly by the start-up of the circuit block. That is, the switch is a 3-state.

4. In the period (4) and later, it disconnects the circuit block from the external, and the circuit block drives through a virtual power supply wire only by the electric charge.

B. *Circuit Block*

The circuit block consists of an op-amp circuit and a reference circuit. Moreover, in order to control the amount of supply a current to the circuit brock as well as to mitigate the noise on a virtual power supply wire, a plug PMOS is introduced between the virtual power supply wire and the circuit brock.

This plug PMOS is designed so that the connectoin from the drain to the source is always a high impedance, and it supplies the electric charge in C to the circuit block only by the leakage current. Moreover, the effect for alleviating the noise of the power supply wire by the capacitor between the drain-source. can be observed The whole proposed system circuit diagram is shown in Figure 7.

IV. Individual Characteristic of Op-amp

In this section, we individually evaluate the op-amp used in the circuit block about the input dynamic range, the through rate, and the DC gain by the simulation.

A. *Input Dynamic Range*

In this evaluation, the op-amp composes a voltage follower as shown in Figure 8. Applying 0V-1.2V to the input, we observe the relation between the input and the output. The verification result is shown in Figure 9. Looking at the result, the input common mode range is 0.1V-1.1V.

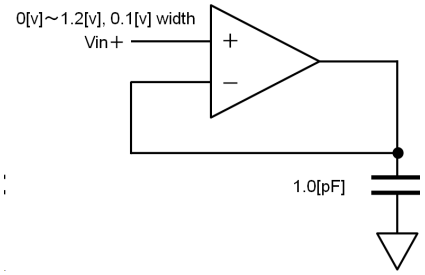

Fig. 8. The circuit for input dynamic range verification

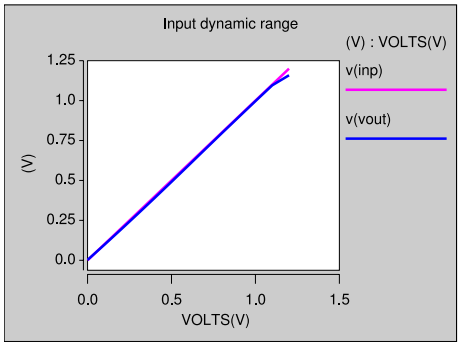

Fig. 9. Input dynamic range

B. *Slew Rate*

As described in [1], the slew rate is an important characteristics to verify the high-speed. The simulation result is shown in Figure 10.

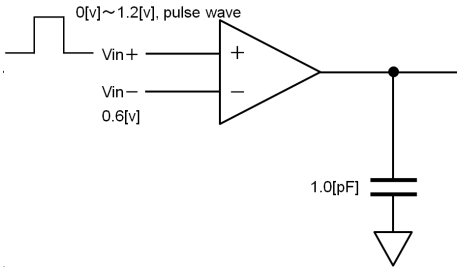

Fig. 10. The circuit for slew rate verification

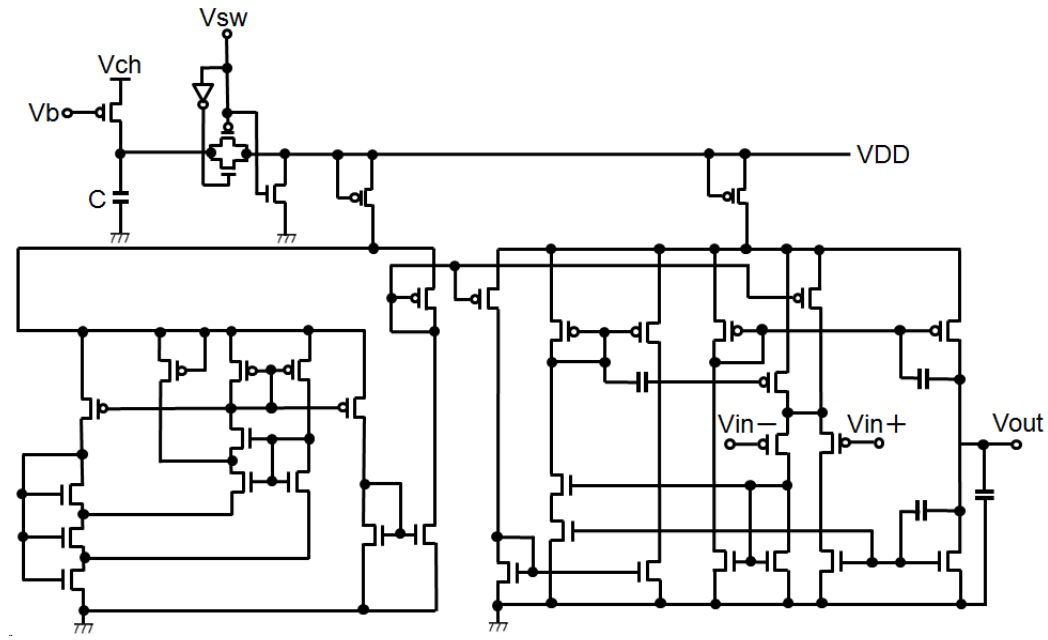

Fig. 7. The whole proposed system circuit diagram with the supply plug PMOS

We define the slew rate such that it is the time for changing the voltage ratio from 10% - 90 %. The raising time of the output is shown in Figure 11.

Observing this figure, the slew rate is calculated as;

$$SR^{+} = \frac{1.0809[V] - 0.1158[V]}{67.694[\mu s] - 62.159[\mu s]} = 0.1743[V/\mu s]$$

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Compared to the result in [1], $SR^{+} = 0.0506[V/us]$ is about 3.4 times more nearly high-speed.

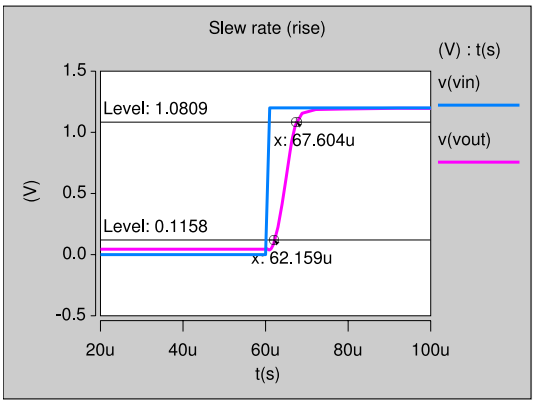

Fig. 11. Slew rate verification (rise)

Next, we evaluate the slew rate when falling. Similarly, the time for the voltage ratio from 10% to 90 % is obtained as;

$$SR^{-} = \frac{1.0804[V] - 0.1203[V]}{307.74[\mu s] - 304.37[\mu s]} = 0.2848[V/\mu s].$$

This is about 4.9 times more nearly high-speed than that in [1].

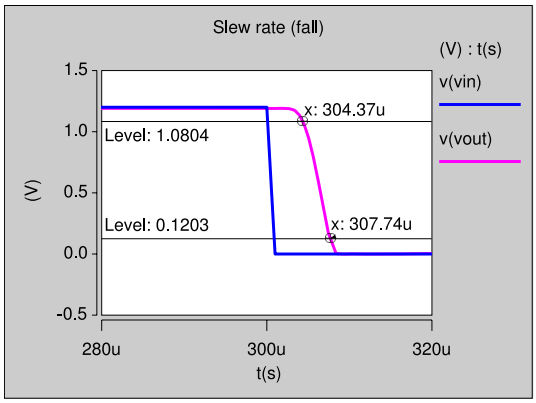

Fig. 12. Slew rate verification (fall)

C. DC Gain

Next, we evaluate the DC gain of the op-amp, and the circuit for the evaluation is shown in Figure 13.

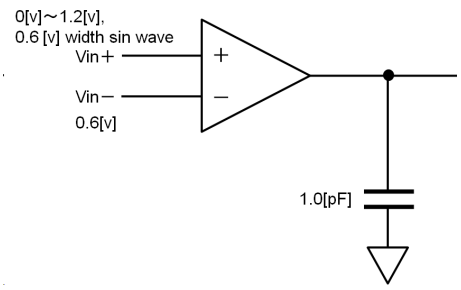

Fig. 13. The circuit for DC gain verification

The simulation result of the gain-frequency curve is obtained as shown in Figure 14. We found that the op-amp has only 7 dB DC gain. In fact, in the preliminary verification of this work, when evaluating the DC gain of an op-amp can be designed so that it has 30 dB for 1.2 V power supply voltage, and 50 dB for 3.3V power supply voltage.

In a proposed system incoporating the op-amp with 30 dB DC gain, however, a current via the plug PMOS is too small to drive the op-amp.

Therefore, in this work, we re-design the op-amp of the low DC gain, and embed it into the proposed system. The DC gain of the op-amp results in 7 dB. Furthermore, although a total current consumption of 30 dB for an hour is 596nA, it decreases 437nA for 7 dB op-amp.

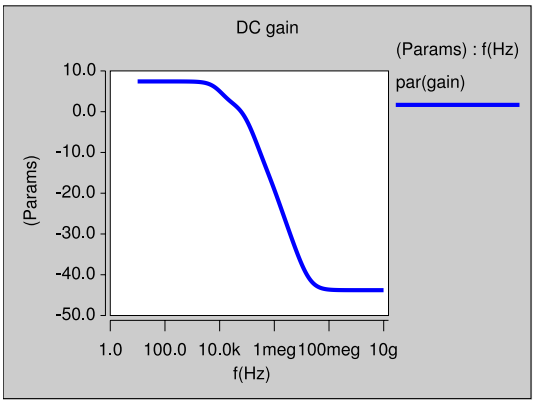

Fig. 14. The verification result of a low gain op-amp

V. Verification of Proposed System

As described in the previous section, the proposed system incorporates the op-amp of the low gain (7 dB) as well as the low current consumption.

In this section, we verify a proposed system according to the following procedures.

1. Only the op-amp is connected to a virtual power supply wire. We assume that the Iref is supplied from the external.

2. Both of the op-amp and the reference circuit are connected to a virtual power supply wire.

A. Verification of Only Op-amp

The circuit working time for the simulation is set to be 1 hour. The transition of the voltage of the virtual power supply wire and the output voltage of the op-amp are shown in Figure 15. The voltage of the virtual power supply wire descends to 1.4V at the time of op-amp starting, and then it becomes mostly stable. The output of the op-amp swings within 0V-1.3V.

The transition of the voltage of the input and output of the op-amp is shown in Figure 16. It is observed that the output follows the input when it changing. As well, it is verified that the circuit works for an hour in the simulation.

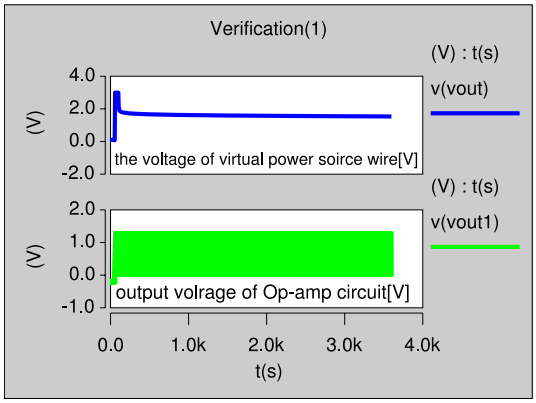

Fig. 15. Verification (1):Transition of the voltage of a virtual power supply wire, and the output voltage of an op-amp circuit

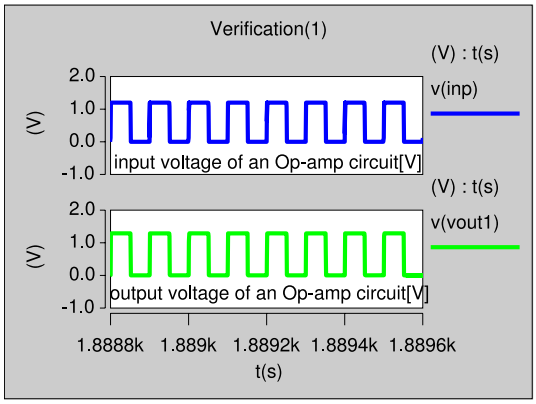

Fig. 16. Verification (1):Transition of the input-and-output voltage of an op-amp circuit

B. *Verification of Reference Circuit and Op-amp*

As the setting in the previous verification, the simulation time is set to be an hour. The transition of the voltage of the virtual power supply wire, and the output voltage of the op-amp are shown in Figure 17. It can be observed that the voltage of the virtual power supply wire descends to 1.4V, and becomes mostly stable as similar to the result shown in Figure 15.

The transition of the voltage of the input and output of the op-amp is shown in Figure 18. We can see that the swing of the op-amp output is within 0V-1.17V, the output follows the input. We attained that the circuit works for an hour in the simulation.

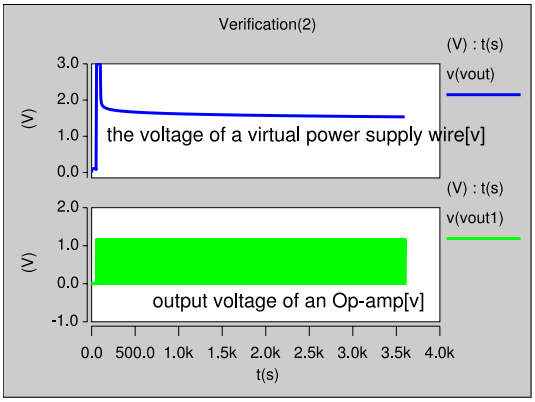

Fig. 17. Verification (2):Transition of the voltage of a virtual power supply wire, and the output voltage of an op-amp

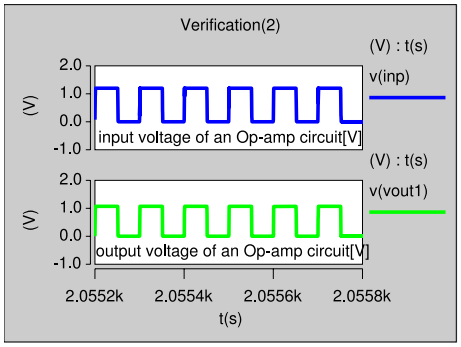

Fig. 18. Verification (2):Transition of the input-and-output voltage of an op-amp circuit

VI. Conclusion

This paper proposed a low-power analog system, where MIM-type on-chip capacitor was used as an independent power supply. The proposed system has the feature which supplies electric power to analog circuit through a virtual power supply wire and the supply plug PMOS. Although it chose on the topic of the super-low-power op-amp as analog circuit and the proposed system was constituted, when an op-amp was designed by high gain, sufficient current supply was not completed from the supply plug PMOS, and it did not operate as a result. Therefore, when an op-amp was redesigned by low gain, operation of the proposed system was able to be checked. In future works, we re-design our proposed system to drive op-amp with a high gain, then apply this system to a sensor IC.

References

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