A Quaternary Master-Slave Flip-Flop with Multiple Functions for Multi-Valued Logics

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Abstract— A prototype of flip-flop circuit is proposed in this work for storing quaternary signals. Inspired by the Neuron-MOS mechanism, the capacitance-coupling technology is implemented to realize multi-threshold inverters. On the basis of this technology, a self-lock feedback scheme is proposed to process and store quaternary signals with standard CMOS technology and ordinary dual-rail supply voltage. Thanks to the inherent property of quaternary processing and proposed scheme, various behaviors can be easily achieved without additional combination-circuits. An example is given on the quaternary counter with sixteen states. From circuit simulation results, the proposed quaternary multi-functional flip-flop achieves all the basic and extended functions correctly.

I. Introduction

Along with the road-map of scaling down, very large scale integrated (VLSI) circuits contain more and more devices on chip. The interconnection explosion appears serious in the development of high-performance VLSI architectures. The great increase of interconnection does not only demand a large number of pins, but also lead to plenty of parasitic effects, which seriously deteriorate the performance of VLSI circuits [1]. These effects do not decrease along with scaling down, but might increase due to compacter on-chip space and package. Even, the interconnection problem is considered as one of the bottleneck of VLSI development [2]. The binary processing, which has been widely applied in VLSIs, benefits us on design convenience and reliability for many decades. However, different fashions of signal processing are still demanded for binding the signal lines. Therefore, the multi-valued logics (MVLs) was developed for a compact data representation [3, 4]. In MVLs, the signals are represented and processed in the form of multiple levels of states. For instance, while four stable levels of signal states are considered, it is called quaternary representation. So far, the VLSI implementations of MVLs have been proved well-performance over capacity, chip size, speed and power dissipation [5, 6].

In fact, there have been many attempts on developing quaternary combinational circuits for signal processing [7, 8, 9] by different schemes. Unfortunately, these efforts were made for a small scale of logic operation instead of complex functions. Considering some more complicated tasks, quaternary sequential circuits are very important in which the quaternary memory unit plays a key role. Several recently reported works were made for the quaternary flip-flop developments [11, 12]. However, special devices (such as single-electron transistor [11]) and multiple supply-voltage lines are always necessary in these works. In this sense, additional interconnections are introduced into chips. Namely, this strategy partially losses the benefit of quaternary processing.

The purpose of this work is to propose a prototype of quaternary flip-flop in the standard CMOS technology and ordinary dual-rail supply voltage lines. By mimicking the Neuron-MOS mechanism [10], the capacitance-coupling is adapted to realize quaternary-input-binary-output inverters with multiple switching thresholds. A set of Neuron-MOS inverters and a set of regular inverters in complementary are cross-coupled for a self-lock feedback. In this manner, a basic quaternary flip-flop is designed, which is named as "Q-type flip-flop" (Q-FF in

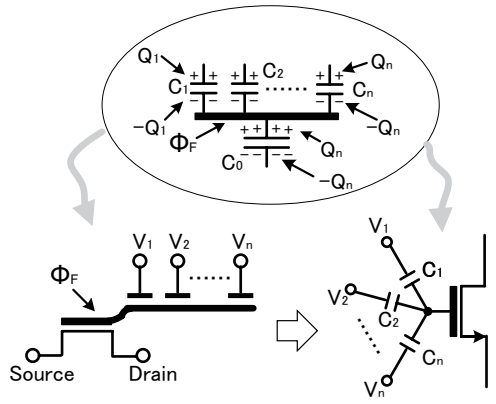
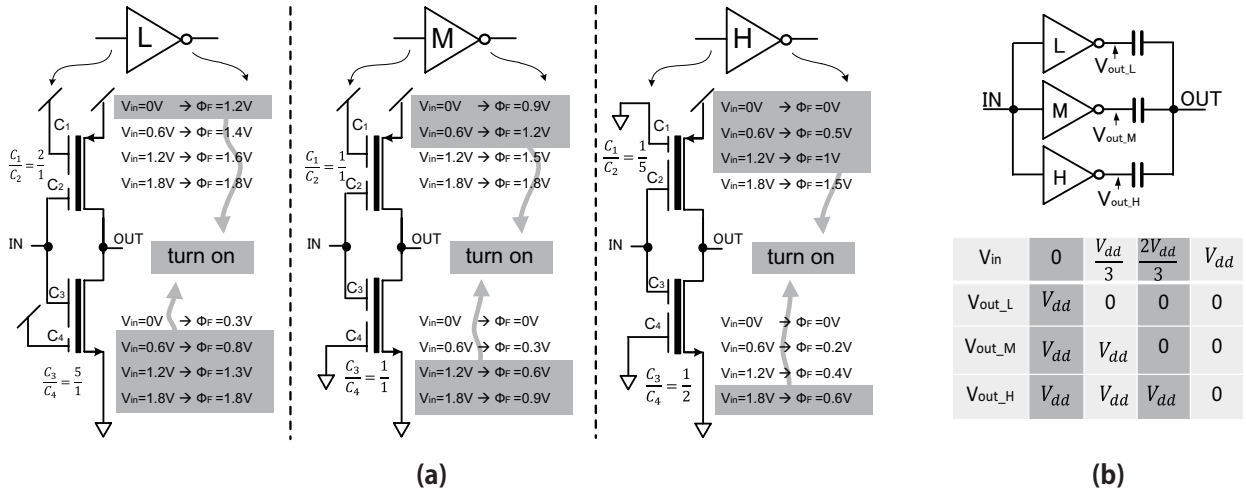


Fig. 1. Structure of Neuron-MOS transistor and its equivalent model by using standard devices (regular MOS transistor and capacitors).



Vin	0	$\frac{V_{dd}}{3}$	$\frac{2V_{dd}}{3}$	V_{dd}
Vout_L	V_{dd}	0	0	0
Vout_M	V_{dd}	V_{dd}	0	0
Vout_H	V_{dd}	V_{dd}	V_{dd}	0

Fig. 2. (a): three types of quaternary-input binary-output inverters are designed with low, middle and high switching thresholds, where the supply voltage $V_{dd} = 1.8V$; and (b): quaternary-input-quaternary-output inverter by capacitance-coupling at the output end.

short) in this paper. Furthermore, it is found that the specific capacitance-coupling schemes give various state representations and functions of flip-flop. In this work, we demonstrate a master-slave Q-FF with exactly following, quaternary-inversing, and quaternary-shifting outputs. By directly connecting two Q-FF, a quaternary counter with sixteen states is designed. From the circuit simulation results, the proposed Q-FF and counter achieve all the expected functions correctly. In general, compared to the previously proposed quaternary flip-flop, our proposed Q-FF is simpler with less supply voltage lines and more flexible functions.

II. Neuron-MOS mechanism and its implementation in MVL circuits

The structure of Neuron-MOS is an n-channel transistor with a gate electrode which is electrically floating [10]. As illustrated in Fig. 1, n input gates are capacitively coupled to the floating gate. The terminal voltages and various capacitive coupling coefficients are defined as $V_1, V_2, \cdots, V_n$ and $C_1, C_2, \cdots, C_n$ respectively, where ϕ_F is the floating-gate potential. The gate capacitance between the floating-gate and substrate is defined as C_0. $Q_0, Q_1, Q_2, \cdots, Q_n$ denote the electronic charges stored on the coupling capacitors. The charge Q_F stored on the floating-gate is calculated as:

$$\begin{aligned} Q_F &= Q_0 + \textstyle\sum_{i=1}^{n} -Q_i = \sum_{i=0}^{n} C_i(\phi_F - V_i) \\ &= \phi_F \textstyle\sum_{i=0}^{n} C_i - \sum_{i=0}^{n} C_i V_i. \end{aligned} \tag{1}$$

It is assumed the no charge injection occurs during device operation (namely, $Q_F = 0$), and the substrate is grounded. Then, the potential on the gate of the MOS transistor can be obtained as:

$$\phi_F = \frac{C_1 V_1 + C_2 V_2 + \cdots + C_n V_n}{C_{TOT}}, \tag{2}$$

where $C_{TOT} = \sum_{i=0}^{n} C_i$. In this paper, we assume the gate capacitance of Neuron-MOS is sufficiently small compared to the terminal capacitors.

The capacitance-coupling technology can be applied in the inverter design as shown in Fig. 2 (a). By adapting specific configuration of capacitance-coupling, the switching threshold of inverters is set as different values. For a quaternary representation, three different thresholds are necessary. Then, three inverters with high, middle, and low threshold are designed. Here, these inverters accept quaternary input but output a binary signal. Adapting the capacitance-couping again at the output end is feasible to generate (or "convert") a respective quaternary signal as illustrated in Fig. 2 (b). In this example, a quaternary-input-quaternary-output inverter is demonstrated. Theoretically, the exact values of capacitance are not concerned; only the ratio among coupling capacitance determines the behavior of the proposed circuit. Thus, the additional capacitors are not chip-area hungry while all capacitors are designed as small values.

In fact, the output of three multi-threshold inverters V_{out_L}, V_{out_M} and V_{out_H} behaves the down literal (DL) function in the form of binary. In this sense, the multi-threshold inverters are considered to convert the quaternary signal into DL codes. The coupling capacitors at the output end convert DL codes back to quaternary signals without any additional supply voltage rail. This technology is the reason that the ordinary dual-rail supply voltage is sufficient for our proposal, instead of four-rail supply voltage in conventional quaternary circuits.

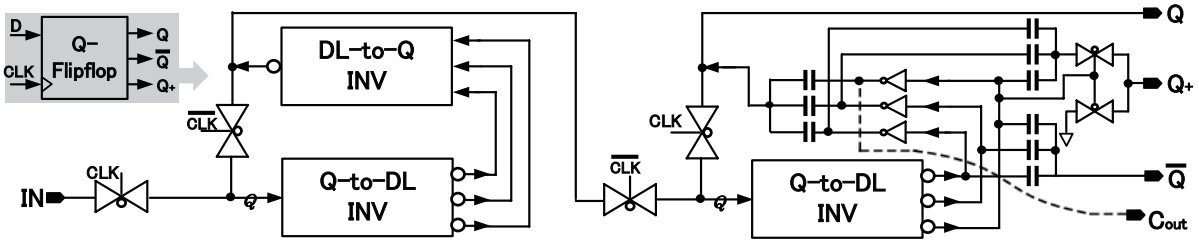


Fig. 4. Master-slave Q-FF is realized by two stage of basic Q-FF, which offers an identical, an inverse, and a shifted output terminal.

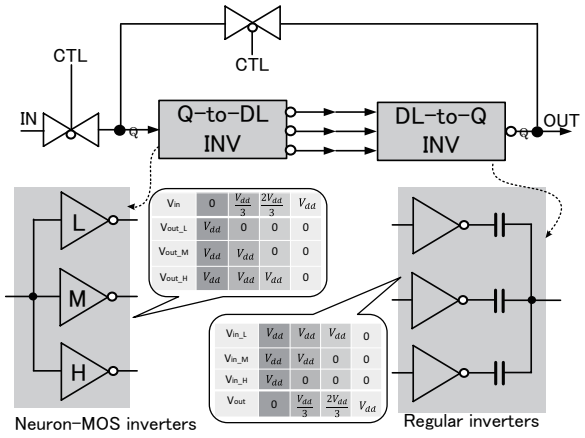


Fig. 3. Two inverters are cross-coupled in the form of flip-flop, which offer self-lock feedback for four stable states.

III. Proposed prototype of quaternary flip-flop

As shown in Fig. 3, the structure of quaternary flip-flop is a pair of cross-coupled inverters mimicking the binary flipflop prototype. At the first stage, three multi-threshold inverters (Neuron-MOS inverters) inversely encode the quaternary input into the DL codes. It is named "Q-to-DL" inverter. The second stage is a set of three regular binary inverters with capacitance coupling at the output end, which is complementary to the first stage. It is called "DL-to-Q" inverter. In this manner, four stable states are available and reliably stored without refreshing. Here, four levels of quaternary states "0", "1", "2", and "3" are represented by voltages 0, $\frac{V_{dd}}{3}$, $\frac{2V_{dd}}{3}$, and V_{dd}, respectively.

This prototype of quaternary flip-flop is named "Q-type Flip-Flop" (Q-FF in short) by this work. Here, the basic Q-FF is triggered by the edge of control signal "CTL". The stored signal is transparent to the input in the phase of high voltage of "CTL". The behavior of Q-FF is comparable to conventional D-type binary flip-flop; the storage directly reflects input triggered by the edge of control signal. Regarding the number of devices, Q-FF consists of six inverters and two CMOS switches (namely, 16 transistors). To realize a similar two bit binary D-flipflop, four inverters and four CMOS switches are necessary (16 transistors). In this sense, their chip areas are similar.

IV. Master-slave Q-FF with various functions

As mentioned above, the essence of proposed structure is a complementary encoding/decoding between DL logic and quaternary representation. Inner the Q-FF, there are three outputs at the output end of "Q-to-DL" inverter and other three at the output end of "DL-to-Q" inverter. The choice and combinations of specific coupling terminals offer plenty of different behaviors. Therefore, the proposed Q-FF has a potential to carry out various functions for different tasks. Namely, Q-FF itself could perform complexer functions than a binary flip-flop since it plays the role of not only flip-flop but also combinational circuits.

Here, a master-slave Q-FF with three output states is presented for proof-of-concept as shown in Fig. 4. The basic structure emulate the binary master-slave flip-flop. However, at the output stage, three different coupling scheme is adapted as follows:

1. Q: capacitance-coupling at the output end of last "DL-to-Q" inverter generates the identical storage signal;

2. $\bar{Q}$: capacitance-coupling at the output end of last "Q-to-DL" inverter generates the inverse storage signal. The quaternary values "0", "1", "2", and "3" are converted to "3", "2", "1", and "0", respectively;

3. Q_+: two DL signals from "DL-to-Q" and one from "Q-to-DL" are coupled by capacitance. This output is the "+1 shifted" value of storage signal. The quaternary values "0", "1", "2", and "3" are shifted to "1", "2", "3", and "0", respectively.

4. C_{out} (optional): one output of "Q-to-DL" inverter is wired out. Obviously, this signal is not quaternary but binary for a potential use as trigger (active in the case study in the rest part of this paper). Among four states of stored signal, only one ("3") activates C_{out}.

In this demonstration, three output terminals are active. It is easily extended for more one-quaternary-bit logics depending on the real-world applications.

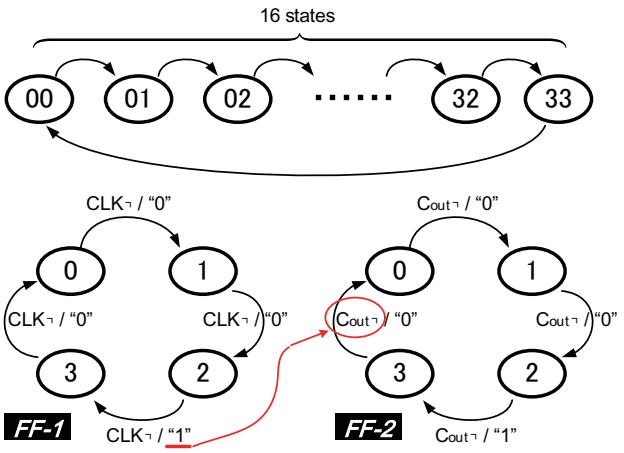


Fig. 5. Finite state machine of quaternary 16-state counter.

V. Case study: sixteen-state counter

To investigate the feasibility for the proposed Q-FF to apply in the sequential circuits, a case study is made for sixteen-state counter. Our target is to carry out practical quaternary functions without the support of combinational circuits. In this manner, the extension of states only employs more Q-FFs but not changes the design at the combinational end (regarding the conventional binary approaches).

As illustrated in Fig. 5, sixteen states in quaternary logic call for two bits quaternary signals instead of four bit binary. The full finite state machine (FSM) is divided into two parts for two Q-FFs. The carry over signal mentioned above is introduced to the second Q-FF as a control trigger. The circuit implementation is presented in Fig. 6. Two Q-FFs are directly connected without combinational circuitry paths. The carry over terminal of the first Q-FF is fed to clock trigger of the second Q-FF; the "Q_+" output of each Q-FF is fed back to the input terminal of itself. Then, on every "CLK" edge of Q-FF1, its state is updated by adding quaternary "1". The same mechanism operates on Q-FF2, which is triggered by carry over index of Q-FF1 instead of "CLK". After an entire state loop, both Q-FFs return to the start state. They behave full sixteen states of 16-counter with carry over index. The "Q" terminals for both Q-FFs are wired out to represent the current state of entire counter circuit.

Regarding the extension of state, arbitrary number of Q-FFs is directly connected in chain. Since no any combinational circuit is employed, the structure of circuitry is constant. It is an important benefit for practical applications because the design of quaternary combinational circuits is always a great challenge.

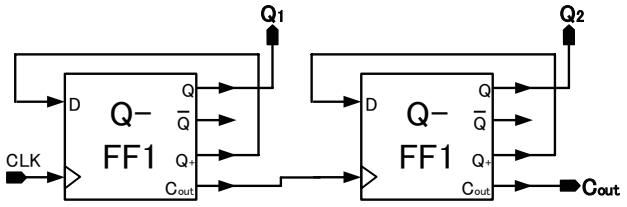


Fig. 6. Two Q-FFs are directly connected without combinational circuitry paths. They behave full sixteen states of 16-counter with carry over index.

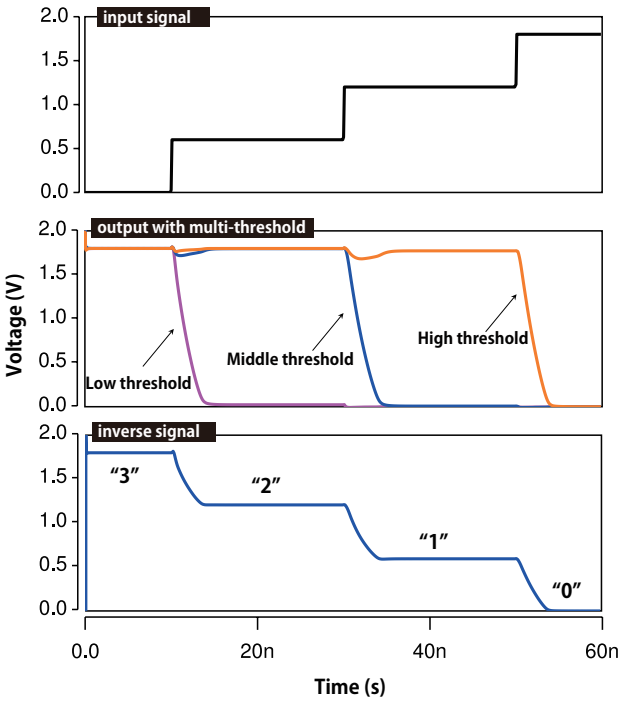


Fig. 7. Three different switching threshold of inverters are achieved for quaternary processing. By coupling their outputs, a quaternary signal (inversion in this case) is generated.

VI. Circuit simulation results

For proof-of-concept, all the proposed circuits are simulated in a standard 0.18μm CMOS technology. In these experiments, the supply voltage is set as 1.8V. Namely, the quaternary values "0", "1", "2", and "3" are represented by 0, 0.6V, 1.2V, and 1.8V.

A. Neuron-MOS inverters and quaternary inverter

Considering the quaternary representation, three different switching thresholds are necessary. From the simulation results in Fig. 7, three Neuron-MOS inverters flip at different thresholds to distinguish four levels of input voltage. By a simple capacitance-coupling at their output end, a inverse quaternary signal is successfully generated.

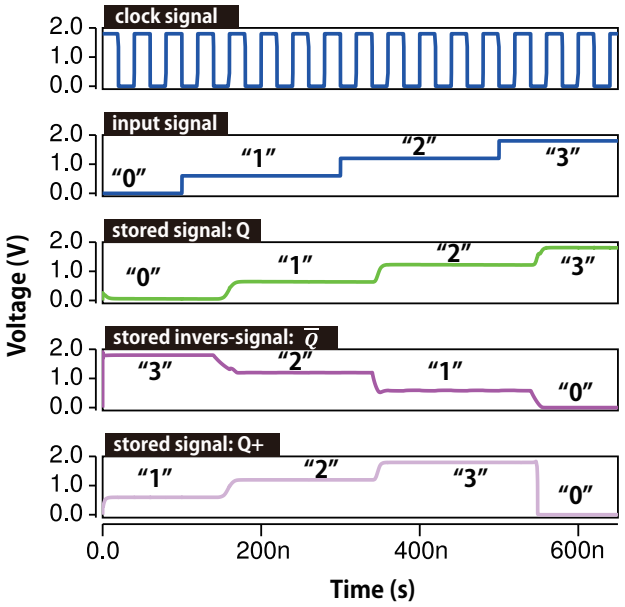


Fig. 8. When a clock is used as control signal, one-bit quaternary input data is stored in Q-FF with three state representations: "Q" is identical to input; "$\bar{Q}$" is inverse to input; and "Q_+" is plus-one shifted to input.

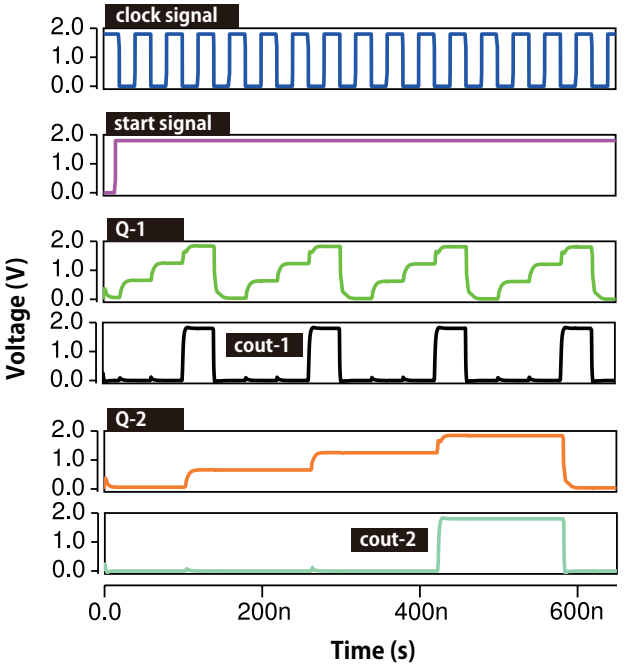


Fig. 9. Sixteen-state counter is verified by investigating the state of two Q-FF in chain.

B. *Behavior of proposed Q-FF*

The behavior of proposed master-slave Q-FF is verified by simulation results as shown in Fig. 8. A clock with $25MHz$ is applied as control signal. The input signal is manually defined with four states for full investigation of one-bit quaternary data. From the simulation results, the data is successfully stored at every falling edge of clock. The "Q" output exactly reflects the stored state; "$\bar{Q}$" reflects the inversion of stored state; and "Q_+" outputs a quaternary data with plus-one shifted value of input.

C. *Sixteen-state counter*

As a case study, the sixteen-state counter is also simulated. This circuitry counts the number of clock falling edges till sixteen edges are detected. In this experiment, a "start" signal is introduced to control the start point of counting period. Combination between states of two Q-FFs Q_1 and Q_2 indicates all sixteen states of entire circuitry. The carry over signal C_{out1} of first Q-FF flips once when clock falling edges come for four times; it gives the second Q-FF a trigger signal at the same time. The carry over signal C_{out2} of the second Q-FF flips only if the clock edges come for sixteen times. Then, C_{out2} is counting termination index of entire counter. From the simulation results in Fig. 9, the proposed counter executes the counting task correctly and return to the initial state successfully. From the viewpoint of function, this quaternary counter performs as exactly same as binary counter with four flip-flops, but in the form of quaternary fashion. Namely, the number of flip-flops and interconnections are reduced to half and same even more flexible functions are achieved. It offers a convenient use when a complex quaternary processor is designed.

VII. Summary and Conclusions

A quaternary flip-flop is proposed for the direct use in quaternary sequential circuits, which is originally named Q-FF by this work. By employing the Neuron-MOS-like mechanism, the prototype of static storage for quaternary signals is realized with standard CMOS technology and ordinary dual-rail supply voltage. Moreover, due to the property of proposed scheme, various and flexible functions can be achieved by a single flip-flop. A sixteen-state counter is designed with two Q-FFs but no combinational circuit for proof-of-concept. From the circuit simulation results, the proposed Q-FF behaves all the investigated functions correctly.

Acknowledgements

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