

IC Design Challenges and Opportunities in Advanced Process Nodes

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Abstract

Moore's Law has entered a new frontier as the incessant pace of device scaling continues to approach 10nm and beyond. As the physical dimension of devices and interconnect are shrunk, the design rules and the design flow, both ASIC and custom designs, face unprecedented complexity. Hence, common IC design practice can no longer separate the design and the process fabrication indifferently. Conventional design optimization techniques also need to take the novel process technologies, such as multi-gate devices (e.g., FinFET), spacer technology, and self-aligned multiple patterning lithography, into account in order to achieve the best possible performance, power, and area. In this talk, I will touch upon the challenges and implication of these new process technologies to IC designers from the foundry's perspective and show how and what to innovate in EDA tools for bridging the gap between physical design and foundry fabrication, and then finally improve the overall design productivity.