Prototype Speed Limit Sign Recognition System Implementation on Rapid Prototyping Platform

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Abstract - This paper introduce our prototype speed limit traffic sign recognition system implementation on Rapid Prototyping Platform. The system utilizes simple image feature such as area luminosity difference of grayscale image to detect traffic sign candidates and block histogram feature in binary image to recognize the speed. Combination of those simple traffic sign features helps our algorithm to achieve 100% of accuracy in recognizing speed limit traffic signs in daytime and over 90% in hard lightning condition such as rainy night. Simplicity in computation enables real-time processing (> 30 fps) and relatively small hardware occupied. The design occupies 11,713 slices LUTs (0.95%) and 5,060 slice registers (0.2%) of the hardware available on the Virtex xc7v2000t (1,221,600 slice LUTs and 2,443200 slice registers) on the Rapid Prototyping Platform Protium.

I. Introduction

The traffic sign recognition is very important in the Advance Driver Assistance System (ADAS) because it support the driver to recognize the potential dangers such as over speed and dangerous road.

The most important of a car assistant system is to improve the driver's safety and comfort. An assistant system with speed limitation recognition ability can inform the driver about the change in speed limit as well as notify them if they drive at over speed. The traffic sign itself faces with recognition problems such as LED sign, image sign taken in rainy night, backlighting sign, and incline sign. Several researches on traffic sign detection system have been given on both hardware and software but all have problems on recognition speed, and so difficult to apply to real time processing (15 ~ 30 fps).

In this study, we introduce a real-time speed limit sign recognition system, which can correctly recognize speed limit sign even in distortion situations such as inclined, underexposure and overexposure signs. It is also usable in many countries such as Japan or German. The platform can be used with high/low resolution, grayscale/color camera. Even the prototype platform is implemented on high-end Virtex 7 in Rapid Prototyping Platform Protium, it is adaptable to low-end low-cost automotive FPGA such as Zynq system. The implementation requires no CPU as well as no complex logics such as multiplier/ divider. Hence, it occupies very small hardware size. The implementation, debug and verification of the algorithm separately with the interface on Rapid Prototyping Platform Protium also help us in reducing development time for prototyping system.

Our approach roughly detects sign candidates using simple global luminosity difference and local pixel direction voting, and then recognizes number inside using block histogram. Combination of those simple and efficient features generates a 98% accuracy speed limit traffic sign recognition system with dataset taken in Japan.

II. Related Works

A general feature of traffic signs is color, which is predetermined to ensure they get the driver's attention and can be used as a feature in image segmentation [2]. This method required color camera, more computational resources and have recognition difficulty when the color has changed due to age and lighting conditions. Shape of the signs such as a circle can be detected by Hough transform together with edge detection [1]. It is robust to changes in illumination, but requires complex computation. Machine learning based method [2] using scale invariant feature transform together with support vector machine (SVM) or random forest is also applicable. They can process 10-28 fps and achieved 90% in accuracy but faced the color problem in their implementation.

III. Speed Limit Traffic Sign and Recognition System using Simple Features of Traffic Sign

Fig. 1 shows the algorithm and implementation of speed limit traffic sign recognition system using simple traffic sign features [3] on Protium. The traffic sign candidates in rectangle and circle forms are detected using area luminosity feature of scan window in a grayscale image, resulting location and size of candidates. Then, the detected candidates are block histogram and circle detection processed in parallel on their binary image and compared with pre-defined feature of number and circle with corresponding size. Binarization process can be done either on software (blue path) or

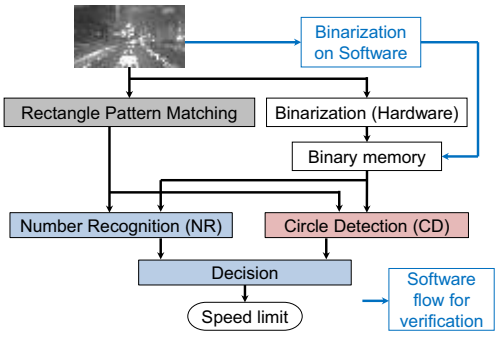

Figure. 1 Hardware / software co-design system implementation for speed limit traffic sign recognition algorithm based on simple features of traffic sign

hardware depending on verification stage. Finally, results from NR and CD are combined for final result. The pre-defined block histogram and circle features can be changed to match the font of different countries.

IV. Prototype Speed Limit Traffic Sign Recognition System Implementation and Verification on Rapid Prototyping Platform Protium

Rapid Prototyping Platform Protium developed by Cadence [4] allows developer to simultaneously develop hardware and software by a unique compile flow as shown in Fig. 2. It includes hardware and an integrated software for compilation, partitioning, interface integration and place and route. It allows developers partition their design, generate their memory in the prototype system without worrying about memory hierarchy, interface and synchronization. Developers can monitor and control signals during execution.

Fig. 3 shows our prototype hardware / software co-design speed limit traffic sign recognition system implemented on Protium. The system includes the hardware / software communication interface on the left and the speed limit traffic sign recognition modules on the right. They work together via Advanced Microcontroller Bus (AXI) and memories.

The communication hardware utilizes various IPs available in Xilinx design library such as PCIe, CDMA, AXI bus, and BRAM in design to reduce the development time. Core of the speed limit sign recognition system includes rectangle pattern matching (RPM) and number recognition is developed and runtime debugged using Cadence Protium software

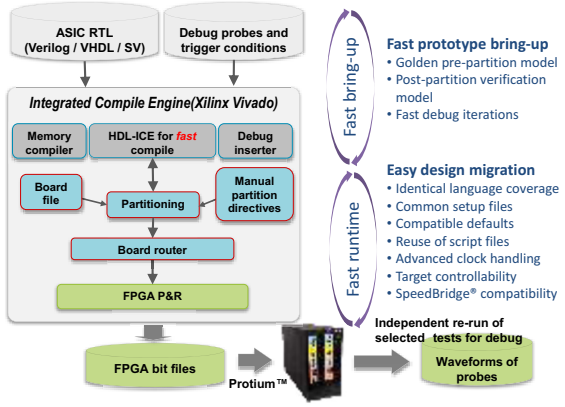

Figure. 2 Protium Compile Flow [4].

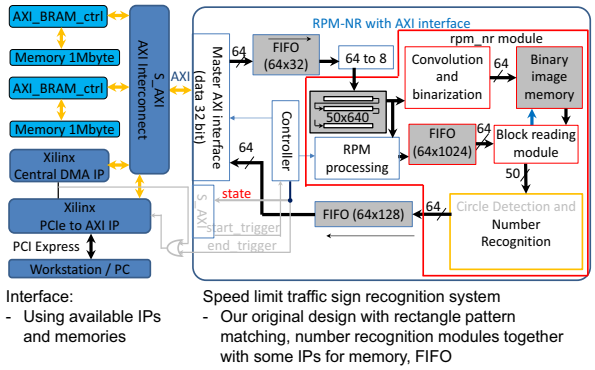

Figure. 3 Prototype Speed Limit Traffic Sign Recognition System Implementation on Protium.

Table 1. Hardware occupied on Protium system.

Virtex 7	No. slice registers	No. slice LUTs	Freq.
Whole system	39,144 / 2,443,200 (1.6%)	49,985/ 1,221,600 (4.09%)	62.5 MHz
RPM-convolution	4,040 / 2,443,200 (0.16%)	6,527 / 1,221,600 (0.53%)	_
NR*	642 / 2,443,200 (0.02%)	2,690 / 1,221,600 (0.22%)	_

xeCompile. The core connects with the interface via a self-developed master AXI interface so that it can read and write data to the memories.

Table 1 shows the hardware occupied by our prototype system on Virtex 7 2000T FPGA, which is used inside Protium hardware. The system takes less than 5% of the hardware available in a single FPGA, and so allows other applications to be implemented. The system works at 62.5 MHz and be able to process over 30 Full HD fps, and so real-time processing.

The algorithm is verified using Japan dataset with 125 scenes taken in day, night, and rainy night and in highway and local roads. It achieves 100% of accuracy in traffic sign candidate detection but reduces to 98% with number recognition integrated.

V. Conclusions

This paper shows our novel algorithm and prototype system for speed limit traffic sign recognition on Rapid Prototyping Platform Protium. Advantage of the integrated software of the Proium helps to reduce prototype system development time by hardware/software development in parallel as well as separately develop the hardware/software interface and our own algorithm. Implementation of the core occupies as small as 1% of the target Virtex 7 FPGA on Protium. The algorithm achieves 98% in accuracy even in hard situation as rainy night scenes. Simplicity in the algorithm and logic also allow our system processes images in real-time regardless the platform.

Acknowledgements

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