SASIMI 2016

Please download onsite proceedings via wireless servers

THE 20TH WORKSHOP ON SYNTHESIS AND SYSTEM INTEGRATION
OF MIXED INFORMATION TECHNOLOGIES

October 24-25, 2016, Kyoto Research Park, Kyoto, Japan

In cooperation with: IEEE Council on Electronic Design Automation (CEDA)
IEEE Circuits and Systems Society (CAS), Kansai Chapter
IEEE Computer Society (CS), Kansai Chapter
The Institute of Electronics, Information and Communication Engineers (IEICE)
Information Processing Society of Japan (IPSJ)

Supported by: The Murata Science Foundation
Kyoto City and the Kyoto Convention & Visitors Bureau

Workshop Program

October 24, 2016

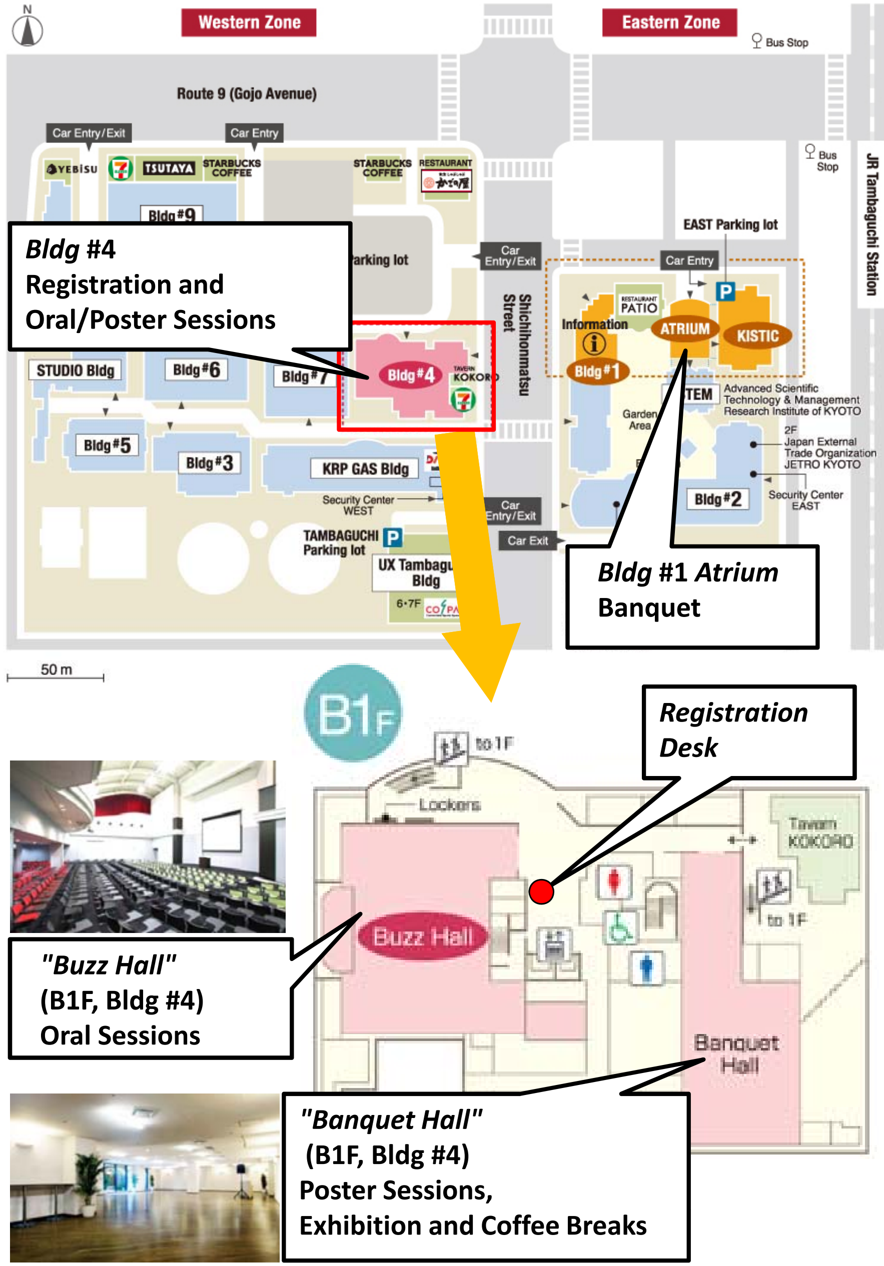
9:00-9:20	*Opening* *(Buzz Hall)*
9:20-10:20	*Keynote Speech (Buzz Hall)* (Chair: Nagisa Ishiura (Kwansei Gakuin Univ.)) Giovanni De Micheli (EPFL, Lausanne, Switzerland) **"Cyber-Medical Systems: Requirements, Components and Design"**
10:20-11:50	*Poster Session I (Buzz Hall/Banquet Hall)* (Co-Chairs: Yoshinori Takeuchi (Osaka Univ.), Kazuya Tanigawa (Hiroshima City Univ.))
11:50-13:20	Lunch Break
13:20-14:10	*Invited Talk I (Buzz Hall)* (Chair: Mineo Kaneko (JAIST)) David Chen (ARM, China) **"Computing in the IoT Era, Opportunities and Challenges"**
14:10-15:40	*Poster Session II (Buzz Hall/Banquet Hall)* (Co-Chairs: Masato Inagi (Hiroshima City Univ.), Seiya Shibata (NEC))
15:40-15:55	*20th Memorial Ceremony (Buzz Hall)*
15:55-17:40	*Memorial Panel Discussion (Buzz Hall)* **"Past and Future 25 Years of Synthesis and System Integration"** Moderator: Isao Shirakawa (University of Hyogo) Panelists: Giovanni De Micheli (EPFL, Switzerland), Youn-Long Lin (National Tsing Hua University, Taiwan), Ren-Song Tsay (National Tsing Hua University, Taiwan), Peter Marwedel (Technical University of Dortmund, Germany) Organizer: Nagisa Ishiura (Kwansei Gakuin Univ.)
18:00-20:00	*Banquet (Atrium)*

20th Memorial SASIMI

October 25, 2016

9:10-10:00	*Invited Talk II (Buzz Hall)* (Chair: Kiyoharu Hamaguchi (Shimane Univ.)) Alan Mantooth (University of Arkansas, U.S.A.) **"Wide Bandgap Analog and Mixed-signal IC Design for Advanced Power Electronics"**
10:00-11:50	*Poster Session III (Buzz Hall/Banquet Hall)* (Co-Chairs: Wenxing Zhu (Fuzhou Univ., China), Hideki Takase (Kyoto Univ.))
11:50-13:20	Lunch Break
13:20-14:10	*Invited Talk III (Buzz Hall)* (Chair: Kiyoharu Hamaguchi (Shimane Univ.)) Ren-Song Tsay (National Tsing Hua University, Taiwan) **"The Challenges and Future of Electronic-System Level Design Automation"**
14:10-16:00	*Poster Session IV (Buzz Hall/Banquet Hall)* (Co-Chairs: Tsuyoshi Matsumoto (Ishikawa Tech. College), Xin Jin (Tsinghua Univ., China))
16:00-16:50	*Invited Talk IV (Buzz Hall)* (Chair: Mineo Kaneko (JAIST)) Takashi Kohno (The University of Tokyo) **"Qualitative-modeling-based design for silicon neuronal networks"**
16:50-17:00	*Closing* *(Buzz Hall)*

Venue Map / Room Assignment



This program is supported by a subsidy from Kyoto City and the Kyoto Convention & Visitors Bureau.

KYOTO
TRADITION MEETS INNOVATION

Day1

Poster Session I

[R1-1] *Detecting Missed Arithmetic Optimization in C Compilers by Differential Random Testing*, Mitsuyoshi Iwatsuji, Atsushi Hashimoto, Nagisa Ishiura (Kwansei Gakuin Univ., Japan)
[R1-2] *Symmetric Segmented Delta Encoding for Wireless Sensor Data Compression*, Shu-Ping Liang, Yi-Yu Liu (Yuan Ze Univ., Taiwan)
[R1-3] *Register-Bridge Architecture and its Application to Multiprocessor Systems*, Takafumi Fujii, Shinichi Nishizawa, Kazuhito Ito (Saitama Univ., Japan)
[R1-4] *Hardware Accelerator of Convolutional Neural Network for Image Recognition and its Performance Evaluation Platform*, Takayuki Ujiie, Masayuki Hiromoto, Takashi Sato (Kyoto Univ., Japan)
[R1-5] *On a Radiation Resistant Data-Path and Controller Synthesis*, Keisuke Inoue (Kanazawa Technical College, Japan)
[R1-6] *A Heuristic Decompositions Index Generation Functions with Many Variables*, Tsutomu Sasao, Kyu Matsuura, Yukihiro Iguchi (Meiji Univ., Japan)
[R1-7] Debugging of Reconfigurable Single-Electron Transistor Arrays, Wen-Chun Zeng, Shih-Hsiang Liu, Yu-Da Chen, Yung-Chih Chen (Yuan Ze Univ., Taiwan)
[R1-8] *Layer Assignment for Multi-Power-Mode 3D IC Designs with Power Distribution Networks Considered*, Shih-Hsu Huang, Jian-Zhi Shen, Chun-Hua Cheng (Chung Yuan Christian Univ., Taiwan)
[R1-9] *A Processor Architecture Integrating Voltage Scalable On-Chip Memories for Individual Tracking of Minimum Energy Points in Logic and Memory*, Jun Shiomi, Tohru Ishihara, Hidetoshi Onodera (Kyoto Univ., Japan)
[R1-10] *CORP: Control Routing for Paper-Based Digital Microfluidic Biochips*, Qin Wang, Hailong Yao (Tsinghua Univ., China), Tsung-Yi Ho (National Tsing Hua Univ., Taiwan), Yici Cai (Tsinghua Univ., China) *Best paper award
[R1-11] *Analysis of Body Bias Control for Real Time Systems*, Carlos Cesar Cortes Torres, Hayate Okuhara, Akram Ben Ahmed, Nobuyuki Yamasaki, Hideharu Amano (Keio Univ., Japan)
[R1-12] *Performance-Driven Multi-Layer OARST Construction with Steiner-Point Pre-Selection and Bounded Maze Routing*, Kuen-Wey Lin, Yeh-Sheng Lin, Yih-Lang Li (National Chiao Tung Univ., Taiwan), Rung-Bin Lin (Yuan Ze Univ., Taiwan), Wen-Hao Liu (Cadence Design Systems, U.S.A.)
[R1-13] *Performance Improvement of General-Synchronous Circuits by Variable Latency Technique using Dynamic Timing-Error Detection*, Shimpei Sato, Hiroshi Nakatsuka, Atsushi Takahashi (Tokyo Inst. of Tech., Japan)
[R1-14] *FPGA Prototyping of a Smart Card Platform for Evaluating Tamper Resistance of Cryptographic Circuits*, Hiroyuki Kanbara (ASTEM RI, Japan), Naoya Ito, Hinata Takebayashi (Kwansei Gakuin Univ., Japan), Muneyuki Takenae (Ritsumeikan Univ., Japan), Takashi Tsukamoto (Information-technology Promotion Agency, Japan)
[R1-15] *Convolutional Neural Network Layer Reordering for Acceleration*, Vijay Daultani, Subhajit Chaudhury, Kazuhisa Ishizaka (NEC, Japan)
[R1-16] *System Design of Vision-based Framework for Senior Driver Assistance*, Eric Aliwarga, Koichi Mitsunari, Jaehoon Yu, Takao Onoye (Osaka Univ., Japan), Toshitaka Azuma, Mitsuhiko Koga (Vehicle Information and Communication System Center, Japan)
[R1-17] *An FPGA Implementation of SVM for Type Identification with Colorectal Endoscopic Images*, Takumi Okamoto, Tetsushi Koide, Tatsuya Shimizu, Koki Sugi, Anh-Tuan Hoang, Toru Tamaki, Bisser Raytchev, Kazufumi Kaneda (Hiroshima Univ., Japan), Shigeto Yoshida, Hiroshi Mieno (Hiroshima General Hospital of West Japan Railway Company, Japan), Shinji Tanaka (Hiroshima Univ. Hospital, Japan) *Outstanding paper award

Poster Session II

[R2-1] *Random Testing of Back-end of Compiler Infrastructure LLVM*, Kenji Tanaka, Nagisa Ishiura (Kwansei Gakuin Univ., Japan), Masanari Nishimura, Akiya Fukui (Renesas System Design, Japan)
[R2-2] *Retention-aware Refresh Techniques for DRAM Refresh Power Reduction*, Wei-Kai Cheng, Po-Yuan Shen (Chung Yuan Christian Univ., Taiwan)
[R2-3] *Stochastic Number Generation with Internal Signals of Logic Circuits*, Naoya Kubota, Hideyuki Ichihara, Tsuyoshi Iwagaki, Tomoo Inoue (Hiroshima City Univ., Japan)
[R2-4] *A Branch-and-Bound Algorithm for Scheduling of Data-Parallel Tasks*, Yang Liu, Lin Meng, Ittetsu Taniguchi, Hiroyuki Tomiyama (Ritsumeikan Univ., Japan)
[R2-5] *Automatic Enable Candidate Extraction for Backward Sequential Clock Gating*, Shinji Kimura, Tomoya Goto, Masao Yanagisawa (Waseda Univ., Japan)
[R2-6] *A Decision Diagram to Analyze Probabilistic Behavior of Circuits*, Kodai Abe, Shigeru Yamshita (Ritsumeikan Univ., Japan)
[R2-7] *Random Delay Elements for Tamper Resistant Asynchronous Circuits based on 2-phase Handshaking Protocol*, Daiki Toyoshima, Tatsuya Ishikawa, Atsushi Kurokawa, Masashi Imai (Hirosaki Univ., Japan)
[R2-8] *Optimization of Temperature Dependent Intentional Skew for Temperature Aware Timing Design*, Makoto Soga, Mineo Kaneko (JAIST, Japan)
[R2-9] *Performance Evaluation Platform for Programmable Interconnect Architecture Exploration*, Kohei Yamamoto, Toshiki Morioka, Tomoya Inoue, Masataka Mori, Yukio Mitsuyama (Kochi Univ. of Tech., Japan)
[R2-10] *Efficient Standard Cell Layout Synthesis Algorithm Considering Various Driving Strengths*, Hong-Yan Su, Bo-Shung Wang, Sin-Ye Hsieh, Yih-Lang Li (National Chiao Tung Univ., Taiwan), I-Hsun Wu, Chang-Chung Wu, Wei-Chiang Shih (M31 Technology, Taiwan), Hidetoshi Onodera (Kyoto Univ., Japan), Masanori Hashimoto (Osaka Univ., Japan) *IEEE CEDA Young researcher award
[R2-11] *Fast Length-Matching Routing for Rapid Single Flux Quantum Circuits*, Nobutaka Kito (Chukyo Univ., Japan), Kazuyoshi Takagi, Naofumi Takagi (Kyoto Univ., Japan)
[R2-12] *A Comparative Study on Multisource Clock Network Synthesis*, Wen-Hsin Chen, Chun-Kai Wang, Hung-Ming Chen (NCTU Taiwan, Taiwan), Yih-Chih Chen, Cheng-Hong Tsai (Global Unichip, Taiwan)
[R2-13] *Target Concentration Exploration for Reactant Minimization on Digital Microfluidic Biochips*, Yi-Ling Chen, Yung-Chun Lei, Juinn-Dar Huang (National Chiao Tung Univ., Taiwan)
[R2-14] *Practical and Accurate SOC Estimation System for Lithium-Ion Batteries by EKF with Adaptive Noise Covariance Estimation*, Lei Lin, Kiyotsugu Takaba, Masahiro Fukui (Ritsumeikan Univ., Japan) *IEEE CEDA Young researcher award
[R2-15] *True Random-Bit Generation Using a Continuous-Time Chaotic Oscillator*, Chatchai Wannaboon, Masayoshi Tachibana (Kochi Univ. of Tech., Japan)
[R2-16] *Hardware Acceleration Technique for Radio-resource Scheduler in Ultra-high-density Distributed Antenna Systems*, Yuki Arikawa, Hiroyuki Uzawa, Takeshi Sakamoto, Satoshi Shigematsu (NTT, Japan)
[R2-17] *An Overlay Architecture for FPGA-Based Industrial Control Systems Designed with Functional Block Diagrams*, Taisei Segawa, Yuichiro Shibata, Yudai Shirakura, Kenichi Morimoto, Hidenori Maruta, Fujio Kurokawa (Nagasaki Univ., Japan), Masaharu Tanaka (Mitubishi Heavy Industries, Japan), Masanori Nobe (Mitubishi Hitachi Power Systems, Japan)

Day2

Poster Session III

[R3-1] *Extending Distributed Control for High-Level Synthesis beyond Borders of Basic Blocks*, Miho Shimizu, Nagisa Ishiura (Kwansei Gakuin Univ., Japan)
[R3-2] *Proposal of an Efficient Clock-Gating Mechanism for Multi-Core Processors to Reduce Power Supply Noise*, Jun Kawabe, Yoshinori Takeuchi, Jaehoon Yu, Masaharu Imai (Osaka Univ., Japan)
[R3-3] *Automatic Netlist Transformation for WDF-Based Analog Emulator*, Hsu-Ping Yang, Hsin-Ju Hsu, Chun Wang, Chien-Nan Jimmy Liu, Jing-Yang Jou (National Central Univ., Taiwan) *IEEE CEDA Young researcher award
[R3-4] *Nonlinear Optimization Solver with Multiple Precision Arithmetic*, Yuya Matsumoto, Hiroshige Dan (Kansai Univ., Japan)
[R3-5] *High Speed Cycle-Accurate Processor Simulation Through Ahead of Time Compilation*, Lovic Gauthier (Ariake National College of Tech., Japan)
[R3-6] *Prototype Speed Limit Sign Recognition System Implementation on Rapid Prototyping Platform*, Anh-Tuan Hoang, Takumi Okamoto, Tetsushi Koide (Hiroshima Univ., Japan)
[R3-7] *Reconfigurable Processor Array Architecture for Deep Convolutional Neural Networks*, Kota Ando, Kentaro Orimo, Kodai Ueyoshi, Masayuki Ikebe, Tetsuya Asai, Masato Motomura (Hokkaido Univ., Japan)
[R3-8] *On Component Ratio of RECON Spare Cells for ECO-Friendly Design Style*, Takeshi Sawai, Ayano Takezaki, Tetsuya Hirose, Nobutaka Kuroki, Masahiro Numa (Kobe Univ., Japan)
[R3-9] *Theorem-proving Verification of Multi-clock Synchronous Circuits on Multimodal Logic*, Shunji Nishimura, Motoki Amagasaki, Toshinori Sueyoshi (Kumamoto Univ., Japan)
[R3-10] *Hardware Trojan Insertion Difficulties into Synchronous and Asynchronous Circuits*, Masashi Imai (Hirosaki Univ., Japan), Tomohiro Yoneda (NII, Japan)
[R3-11] *A Delay Adjustment Method for Asynchronous Circuits with Bundled-data Implementation Considering a Latency Constraint*, Kazumasa Yoshimi, Hiroshi Saito (Univ. of Aizu, Japan)
[R3-12] *Path Grouping Approach for Efficient Candidate Selection of Replacing NBTI Mitigation Logic*, Shumpei Morita, Song Bian, Michihiro Shintani, Masayuki Hiromoto, Takashi Sato (Kyoto Univ., Japan) *Outstanding paper award
[R3-13] *Semi-Automated Analog Placement based on Margin Tolerances*, Eric Lao, Marie-Minerve Louerat, Jean-Paul Chaput (Laboratoire d'informatique de Paris 6, France)
[R3-14] *An Efficient Gaussian Mixture Reduction to Two Components*, Naoya Yokoyama, Daiki Azuma, Shuji Tsukiyama (Chuo Univ., Japan), Masahiro Fukui (Ritsumeikan Univ., Japan)
[R3-15] *Thermal Circuit Identification of Power MOSFETs through In-Situ Channel Temperature Measurement*, Kazuki Oishi, Michihiro Shintani, Masayuki Hiromoto, Takashi Sato (Kyoto Univ., Japan)
[R3-16] *Evaluation of PLL Layouts based on Transistor Array-style*, Atsushi Nanri, Bo Liu, Yuki Miura, Shigetoshi Nakatake (Univ. of Kitakyushu, Japan)
[R3-17] *Single Row Cell Placement Considering Self-aligned Double Patterning*, Ye-Hong Chen, Ting-Chi Wang (National Tsing Hua Univ., Taiwan)
[R3-18] *A Lithium Ion Battery Aging Simulator with Calibration Functions*, Yukinori Hayakawa, Lei Lin, Masahiro Fukui (Ritsumeikan Univ., Japan)
[R3-19] *A Full Charge Capacity Estimation Algorithm for Li-ion Batteries Based on Recursive Least-Squares Identification with Adaptive Forgetting Factor Tuning*, Hironori Ono, Lei Lin, Masahiro Fukui, Kiyotsugu Takaba (Ritsumeikan Univ., Japan)
[R3-20] *A Hardware Architecture to Perform K-means Clustering for Learning-Based Super-Resolution Combining Self-Learning and Prior-Learning Dictionaries*, Daichi Murata, Ayumi Kiriyama, Tetsuya Hirose, Nobutaka Kuroki, Masahiro Numa (Kobe Univ., Japan)
[R3-21] *On-Chip Temperature Sensing using a Reconfigurable Ring Oscillator*, Tadashi Kishimoto, Hidetoshi Onodera (Kyoto Univ., Japan)
[R3-22] *A Shift HSV Algorithm for a Low-Power Monitoring System using an FPGA toward Internet of Things Agriculture*, Kurose Takahisa (Ehime Univ., Japan), Hiroki Nakahara, Shimpei Sato (Tokyo Inst. of Tech., Japan), Tetsuo Morimoto (Ehime Univ., Japan

Poster Session IV

[R4-1] *Mathematical Algorithm Hardware Description Languages for System Level Modeling*, Ryo Hikawa, Ryuji Kishimoto, Takashi Kambe (Kindai Univ., Japan)
[R4-2] *High-Level Synthesis of Embedded Systems Controller from Erlang*, Hinata Takebayashi, Nagisa Ishiura, Kagumi Azuma (Kwansei Gakuin Univ., Japan), Nobuaki Yoshida, Hiroyuki Kanbara (ASTEM RI, Japan)
[R4-3] *A Data Effect Aware Microcomponent-Based Estimation Approach for Accurate System-Level Memory Device Power Evaluation*, Chi-Kang Chen, Hsin-I Wu, Chi-Ting Hsiao, Ren-Song Tsay (National Tsing Hua Univ., Taiwan) *Outstanding paper award
[R4-4] *Analysis of Co-Controlling Voltage/Frequency of Cores and DRAMs of Chip Multi-Processors with 3D-stacked DRAMs for Thermal Management*, Yi-Jung Chen (National Chi Nan Univ., Taiwan), Chia-Lin Yang, Ping-Sheng Lin, Yi-Chang Lu (National Taiwan Univ., Taiwan)
[R4-5] *Introducing Real Constraints in Partitioned ILP-Based Binding in High-Level Synthesis*, Nagisa Ishiura, Yuuki Oosako (Kwansei Gakuin Univ., Japan)
[R4-6] *A Framework for Automatic Generation of Application-Specific FPGA-based SoC*, Tetsuo Miyauchi, Kiyofumi Tanaka (JAIST, Japan)
[R4-7] *Fast Song Searching by Simultaneous Execution of HiFP2.0 and Staged LSH*, Masahiro Fukuda, Yasushi Inoguchi (JAIST, Japan)
[R4-8] *An Error Diagnosis Technique Based on Averaged EPI Values to Extract Error Locations Sets*, Ayano Takezaki, Takeshi Sawai, Hiroyuki Sakamoto, Tetsuya Hirose, Nobutaka Kuroki, Masahiro Numa (Kobe Univ., Japan)
[R4-9] *Minimum Energy Point Tracking under a Wide Range of PVT Conditions*, Shu Hokimoto, Tohru Ishihara, Hidetoshi Onodera (Kyoto Univ., Japan) *IEEE CEDA Young researcher award
[R4-10] *Comparison of Area-Delay-Energy Characteristics between General Purpose Processors and Dedicated Hardwares for Embedded Applications*, Kei Yoshizawa, Tohru Ishihara, Hidetoshi Onodera (Kyoto Univ., Japan)
[R4-11] *Finding Effective Simulation Patterns for Coverage-Driven Verification Using Deep Learning*, Mami Miyamoto, Kiyoharu Hamaguchi (Shimane Univ., Japan)
[R4-12] *Static Timing Analysis of Rapid Single-Flux-Quantum Circuits*, Takahiro Kawaguchi, Kazuyoshi Takagi, Naofumi Takagi (Kyoto Univ., Japan)
[R4-13] *Improved Method of Simulated Annealing for Unreachable Solution Space*, Hiroyuki Nakano, Kunihiro Fujiyoshi (Tokyo Univ. of Agri. and Tech., Japan)
[R4-14] *Application of Monte-Carlo Tree Search to Traveling-Salesman Problem*, Masato Shimomura, Yasuhiro Takashima (Univ. of Kitakyushu, Japan)
[R4-15] *Analog Characterization Module with D/A Converter Configuration*, Daishi Isogai, Bo Liu, Futa Yoshinaka, Shigetoshi Nakatake (Univ. of Kitakyushu, Japan)
[R4-16] *Range Limiter using Connection Bounding Box for SA-based Placement of Mixed-Grained Reconfigurable Architecture*, Takashi Kishimoto (Ritsumeikan Univ., Japan), Wataru Takahashi, Kazutoshi Wakabayashi (NEC, Japan), Hiroyuki Ochi (Ritsumeikan Univ., Japan)
[R4-17] *A Smart Hybrid Memetic Algorithm for Thermal-Aware Non-Slicing Floorplanning*, Jianli Chen, Yan Liu, Ziran Zhu, Wenxing Zhu (Fuzhou Univ., China)
[R4-18] *Hardware Acceleration of Rate-Distortion Optimized Quantization Algorithm*, Yusuke Funayama, Takashi Kambe (Kindai Univ., Japan), Gen Fujita (Osaka Electro-Communication Univ., Japan)
[R4-19] *Development of an Optimal Wireless Power Transfer System for Lithium-Ion Battery Charge*, Yuto Honda, Lei Lin, Masahiro Fukui (Ritsumeikan Univ., Japan)
[R4-20] *Design of a Fast Lock-in and Low-Power All-Digital Frequency Synthesizer with a Wide Tuning Range*, Hao-Chiao Hong, Hung-Yi Wen (National Chiao Tung Univ., Taiwan), Hong-Yi Huang (National Taipei Univ., Taiwan)
[R4-21] *A Method for Recognizing a Breaking Sound of a Window Glass for Realizing a Low-power Security Surveillance System Using FPGA*, Ryo Terafuji, Hiroyuki Ochi (Ritsumeikan Univ., Japan)
[R4-22] *Electromagnetic Analysis for a Lightweight Block Cipher Simon*, Yusuke Nozaki, Yoshiya Ikezaki, Masaya Yoshikawa (Meijo Univ., Japan)