Efficiency Investigation of Capacitors Mounted on Re-distribution Layers for FOWLP

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Abstract— This paper provides insights on effective usage of an emerging decoupling capacitor. Power supply noise is one of the most serious concerns in the modern low voltage integrated circuits. Decoupling capacitors embedded in the re-distribution layers (RDL) are potentially effective to reduce the noise caused by the internal switching. However, the effectiveness of them is easily lost due to the equivalent series inductance and resistance. Here, we construct a post-layout simulation test bench to discuss the effectiveness by evaluating impedance profile as well as transient noise waveform. The experimental results show that the horizontal proximity of the RDL embedded capacitors to the noise source is an important factor to keep the advantage.

I. Introduction

System on-a-chip (SoC) is required to operate at high speed along with low power consumption. To meet the demands, on chip transistors are scaled down, operating at lower power supply voltages. As a result, current density also increases [1]. Fast switching of transistors as well as the high current density produce large voltage drop. The voltage drop affects operation of the circuit as power supply noise [2][3].

Additionally, lower supply voltage relatively lowers the design margin for voltage fluctuations. Therefore, the power supply noise is one of the most serious concerns in the modern low voltage integrated circuits. In order to avoid power supply noise issues, it is necessary to keep impedance on the power distribution network (PDN) seen by the operating transistor less than the target impedance, which determined by the maximum acceptable voltage noise. The target impedance Z_{target} can be calculated as [4]

$$Z_{target} = \frac{V_{dd} \times ripple}{I_{average}} (\Omega) \quad (1)$$

where V_{dd} is a power supply voltage, $ripple$ is the maximum allowable voltage fluctuation. The average current $I_{average}$ is assumed to be 50% of the maximum current. The maximum current I_{max} is calculated from $P = VI_{max}$. Both Power P and supply voltage V are the specified for each SoC. If the PDN impedance is below Z_{target}, the voltage noise will be less than $ripple$.

A typical design approach is to optimize PDN on chip, package and board simultaneously in the frequency domain. It is generally achieved inserting decoupling capacitors [5]. In terms of frequency domain, decoupling capacitors on board, package, and chip cover low, mid, and high frequency regions respectively.

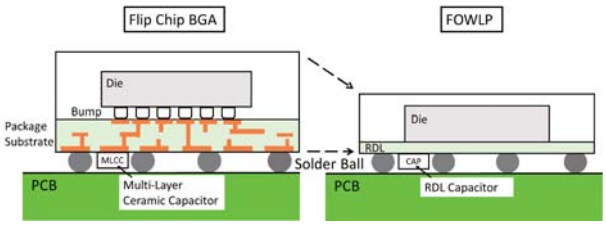

Fig. 1.: Cross sectional comparison of FOWLP with the conventional flip chip BGA.

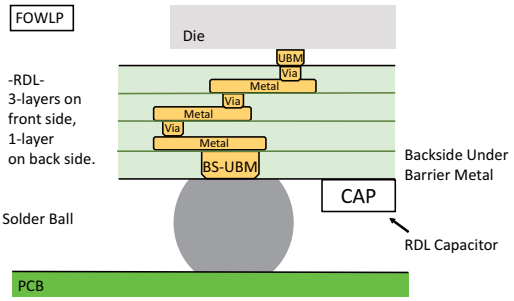

Fig. 2.: Schematic of cross section of RDL wiring.

On the conventional flip chip packages, multi-layer ceramic capacitors (MLCC) are placed near the solder ball. However, the effect of MLCC is limited by the parasitic elements including equivalent series inductance (ESL) and equivalent series resistance (ESR) [6].

In recent years, Fan-Out Wafer-Level Package (FOWLP) which hires re-distribution layers (RDL) instead of the package substrate comes to be adopted for mobile applications [7]. In FOWLP, interconnects are scaled down to the on-chip global routing levels [8]. Fig. 1 and Fig. 2 depict a schematic comparison of the structures and a cross section of RDL wiring.

By placing capacitors directly on RDL, we can reduce ESL and ESR to the same level as the on-chip parasitic elements [9][10]. Besides, decoupling capacitors on RDL are more flexible in placement and analysis compared to the conventional

MLCC. Since RDL can be treated by the same design environments as the on-chip PDN, we can flexibly estimate the decoupling effect of the RDL capacitance to the placement.

In this paper, we experimentally investigate capacitors directly implemented in RDL for a SoC [10]. We show a guideline to effectively implement decoupling capacitors by analyzing the impact of capacitors placement on the PDN impedance as well as corresponding the transient response.

II. PDN Analysis Model

In this section, we provide the details of the PDN analysis model. Fig. 3 illustrates a schematic of a system we assumed. The voltage is supplied by the voltage regulator module (VRM) and delivered to the on-chip PDN through the board and package. Finally, the supply voltage is delivered to the CPU core in the on-chip PDN. Decoupling capacitors for reducing noises are mounted on locations where the board, the package and the chip are.

The goal of this work is to investigate an effective way to implement the decoupling capacitors. For that purpose, we constructed the model that can take into account the dependency of relative positional relationship the decoupling capacitors and the load. The model is compatible with SPICE simulator [11] and then we can evaluate impedance profiles and transient noise waveforms seen by the operating transistor. The individual components of the PDN analysis model are explained in the following subsections.

A. On-Chip PDN Model

On-chip PDN model is constructed referring NanGate 15 nm Open Cell Library [12], Arizona State University (ASU) 14 nm PTM-MG LSTP model (Nominal Vdd = 0.8 V) [13], and North Carolina State University (NCSU) FreePDK15 [14]. The transistor model of FinFET which constitutes a standard cell is based on BSIM-CMG [15].

The path of the on-chip PDN is required to treat as a distributed constant to simulate the dependency of relative positional relationship between the capacitor and the load. Since the ports can be flexibly selected, we use a post-layout netlist. We created an on-chip PDN layout of area 5×5 mm^2 with HVH routing [16] as shown in Fig. 4. TABLE I shows the

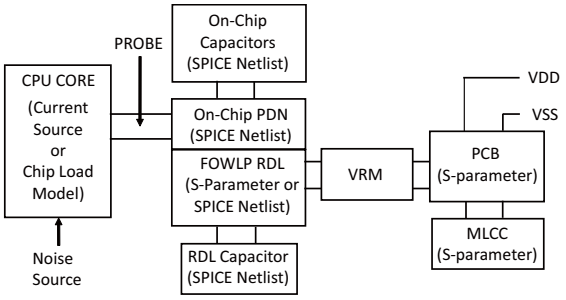

Fig. 3.: Schematic of the analysis model.

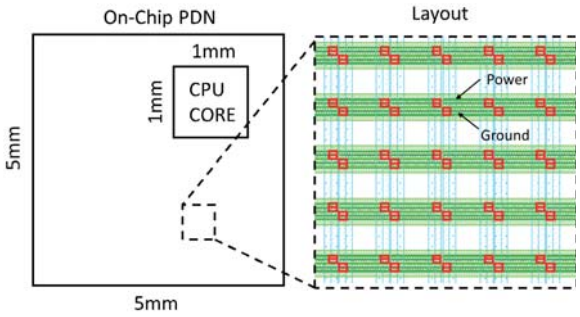

Fig. 4.: The layout of on-chip PDN.

TABLE I
: Parameters of the on-chip PDN model wiring width and pitch.

Layer	Width(um)	Pitch(um)	Direction	Wiring
M1	0.6	0.768	Horizontal	PGPG
M2	15	100	Vertical	P,G pair
M3	15	100	Horizontal	P,G pair
M4	15	100	Vertical	P,G pair
M5	15	100	Horizontal	P,G pair
M6	25	100	Vertical	P,G Pair
M7	25	100	Horizontal	P,G pair

specifications of the wiring width and pitch. From the layout pattern, we obtained the post-layout netlist with a parasitic extraction tool [17]. Summarizing the parasitic extraction, there are 30,778 R elements and 15,993 C elements. In addition, we executed AC analysis the transistor model to estimate on-chip capacitance. The estimated on-chip capacitance 30 nF from chip area were added uniformly to the post-layout netlist.

B. Board and Package Model

We adopted S-parameters obtained from electromagnetic field analysis for board and package models. In particular, FOWLP owns a complicated vertical structure, which tends to cause errors in the analysis results. Therefore, we applied three-dimensional electromagnetic field analysis to ensure causality and passivity in S-parameters [18][19]. The S-parameters of FOWLP include RDL structure. Also, some ports of the models for connecting MLCC are available.

C. Voltage Regulator Module Model

With the progress of voltage reduction, supply voltage is generally supplied to the LSI through a voltage regulator module (VRM). We adopted a switched capacitor integrated VRM which can be implemented on LSI with comparative ease and provides high efficiency [20].

D. Chip Load Model

The chip load model is based on reference [10]. This model takes into consideration the load current response due to power supply voltage fluctuations and the effect on clock delay. In

this work, the chip load model is a 32bit OpenRISC processor synthesized with NanGate 15nm open cell library. The clock frequency for the core processor logic is 1.2 GHz at 0.8 V supply voltage. This model connect to the on-chip PDN model as CPU CORE for analysis of transient response.

E. *Decoupling Capacitor Model*

In this work, the decoupling capacitors that we examine are MLCC on PCB and RDL capacitors. Capacitance of the RDL capacitor is explicitly attached to a port of the package S-parameter. The parasitic component of the RDL capacitor is included in the S-parameter of the package. Both RDL capacitor and MLCC models have the same capacitance value, so that the PDN analysis model considers only the placement dependency of the capacitor.

III. Experimental Results and Discussion

This section describes the experimental results using the PDN model. We calculated the PDN impedance and transient response depending on the location of the capacitors. The PDN impedance is solved by AC analysis with placing 1 A of current source in CPU CORE Fig. 3. The resulted voltage value is read as the PDN impedance. In the transient response calculations, the chip load model is applied to CPU CORE Fig. 3. The observation point commonly for both analyses is located at PROBE.

A. *Comparing effectiveness of RDL capacitor with MLCC*

First, we compare an MLCC mounted on PCB with an RDL capacitor. As shown in Fig. 5, (a) is the position of RDL capacitor, and (b) is the position of MLCC mounted on PCB. Fig. 6 shows the impedance profiles derived by AC analysis. The solid line is the RDL capacitor, and the dashed line is MLCC mounted on PCB. Comparing (a) and (b), we know that RDL capacitor is more effective than MLCC to reduce the PDN impedance in a wide range from 1 MHz to 1 GHz (Here we call the region "middle frequency range"). It is thanks to the advantage of RDL capacitors having a short wiring path to the load. In other words, RDL capacitors accompany less wiring resistance and inductance than MLCC.

Also, Fig. 7 shows the analysis results of transient response of (a) and (b). This analysis ran from 0 s to 125 ns, and the

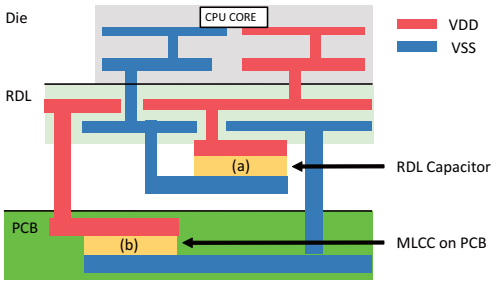

Fig. 5.: Cross section of the on-chip PDN.

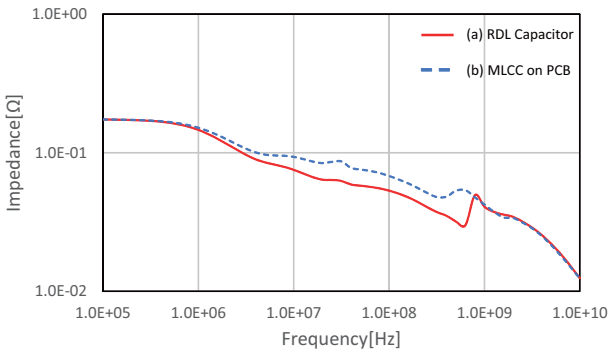

Fig. 6.: Impedance profiles - Comparing RDL capacitor with MLCC on PCB.

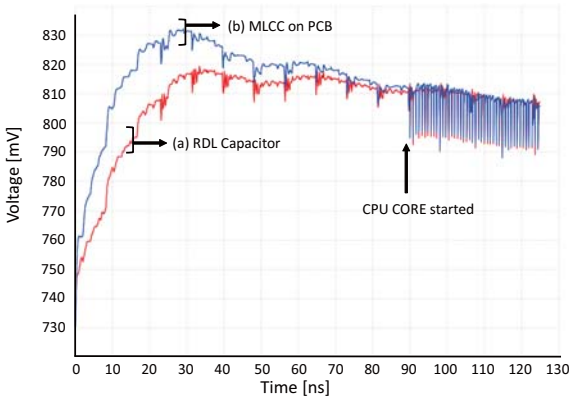

Fig. 7.: Transient waveforms - Comparing RDL capacitor with MLCC on PCB.

operation of the CPU CORE started in 90 ns. The results show that there is an overshoot in the range of 0 s to 50 ns. The overshoot occurred in response to the power supply rise-up including in the middle frequency range. Since (a) has smaller impedance than (b) in the middle frequency range, the overshoot is suppressed.

B. *Dependence of RDL capacitor effectivity on placement*

Next, we demonstrate the location dependence of RDL capacitor. Fig. 8 explains the placement of RDL capacitor. CPU CORE is placed in the upper right area of the on-chip PDN model. Fig. 8 (1) means that the RDL capacitors are placed directly above CPU CORE. This is the same situation as (a) in Fig. 5. Fig. 8 (2) and (3) are the direct neighbor and the diagonal position from CPU CORE, respectively. Fig. 9 shows the PDN impedance profiles of each situation derived by AC analysis. Compared with Fig. 8 (1), Fig. 8 (2) and (3) are less effective in reducing the PDN impedance in the range from 10MHz to 1GHz (upper middle frequency). Larger distance away from CPU CORE causes larger resistance due to on-chip PDN wiring. As a result, the effectiveness of the capacitance is limited.

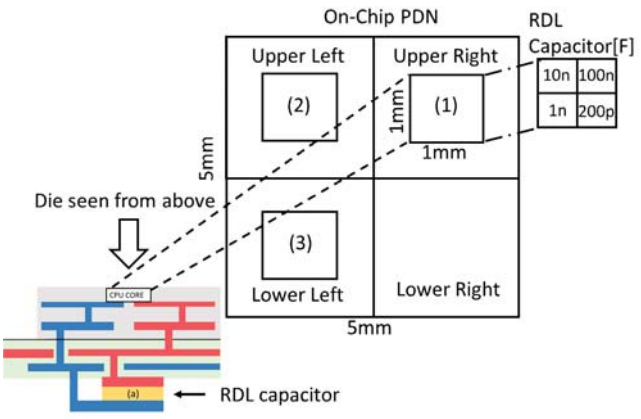

Fig. 8.: RDL capacitor locations.

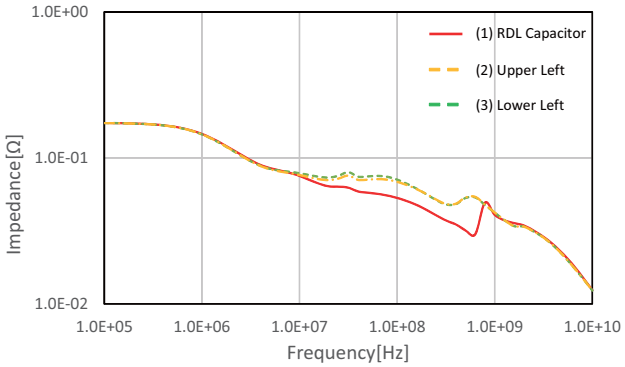

Fig. 9.: Impedance profiles - Dependence on RDL capacitor and CPU CORE placement.

IV. Conclusion

In this paper, we investigated the effective usage of decoupling capacitors to mitigate power noises. We constructed a PDN analysis model to take into account placement dependencies of decoupling capacitors. Then, we experimentally analyzed the PDN impedance profile as well as transient response to evaluate the effectiveness. The results showed that RDL capacitors are more effective than conventional MLCC on PCB. However, even the RDL capacitors, the effect is limited by miss placement. Actually, longer distance from the load CPU eliminates the capacitance effect. From these facts, it is important to implement the RDL capacitor paying attention to the positional relationship with the load.

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