KR-CHIP: An Educational Computer equipped with 8-bit Accumulator-based, 16-bit Accumulator-based and 32-bit Pipeline Processors

Hiroyuki KANBARA Kagumi AZUMA Yuuki OOSAKO* Atsuya SHIBATA†
Wakako NAKANO

ASTEM RI
134 Chudoji Minamimachi
Shimogyo-ku Kyoto,
600-8813, Japan

School of Science and Technology
Kwansei Gakuin University
2-1, Gakuen, Sanda,
Hyogo, 669-1337, Japan

NARA Institute of
Science and Technology
8916-5 Takayama-cho, Ikoma,
Nara, 630-0192, Japan

Abstract— This article presents a processor for computer education named KR-CHIP. KR-CHIP integrates 3 CPUs: 8-bit accumulator-based, 16-bit accumulator-based and 32-bit pipeline architecture. Every register, counter, flag and memory can be observed directly by hardware at any clock cycle or at any phase of instruction execution. KR-CHIP is useful for beginners of computer hardware to understand how instructions are processed inside a CPU.

I. Introduction

IoT (Internet of Things) platform are composed of two types of computing. One is cloud computing, which performs a lot of information processing in a data center. The other is edge computing, which gathers information from sensors and controls external devices like an actuator or a motor.

In the edge side of IoT,there are a wide variety of CPUs from 8 to 32-bit. This is because sensor signal processing capability, real time control requirements and limitation of power dissipation are so many and various. Some IoT devices are equipped with a Linux-supported 32-bit CPU for communication through the Internet. Still simple CPUs are better for sensing or controlling in the edge side because of its low power consumption and cost. Architecture of CPUs in the edge side of IoT may become diverse more and more for optimizing cost performance. How to master operating principle and programming skills of various kinds of CPUs will be an issue now and in the future.

A textbook by Patterson and Hennessy explains a modern 32-bit 5-stage pipeline processor in detail. It is not easy for beginners who are not familiar with MIPS32 instruction set to understand how pipelining mechanism works well. A CPU with simple instruction set and based on accumulator-based architecture is better for beginners of computer hardware to understand instruction execution mechanism through bare-metal programming.

In computer courses at universities, single board computers like Raspberry Pi or Arduino are often used as a teaching material. Students learn programming with C or Python languages using these computers. Both single board computers are easy to program with Linux OS or Arduino IDE (Integrated Development Environment) support. These various layers of abstraction makes bare-metal programming difficult.

Under such background, we have designed CPUs and single board computer system named KR-CHIP. KR-CHIP includes 3 types of CPUs as follows.

- KUE-CHIP2（8-bit accumulator-based）
- KUECHIP-3F（16-bit accumulator-based）
- RUECHIP2 (32-bit pipeline）

These CPUs are specially designed for computer education courses at universities. The biggest feature of KR-CHIP is that users observe how instructions are executed in these CPUs. This will help students to understand the operating mechanism of instruction execution in a CPU core.

The printed circuit board for KR-CHIP possesses a hex keypad for editing main memory contents, a display indicating value of registers or flags within each CPU core and push/toggle switches for program execution control. Students who have acquired how to use this board computer equipped with KR-CHIP can master programming and operating principle of 3 different CPUs easily. The university that introduced the KR-CHIP board computer can plan 3 types of student training course with no extra cost.

This paper describes the purposes of developing KR-CHIP, specification of CPUs of KR-CHIP and its FPGA design.

[*] Currently with GREE, Inc.

[†] Currently with Fixstars Corporation.

II. KUE-CHIP2 and KUECHIP-3F CPU

A. Outline

KUE-CHIP2 is an 8-bit accumulator-based CPU for computer education [1][2][3][4]. Two major purposes of developing KUE-CHIP2 are :

- To make a custom CPU which is useful as teaching materials, for students to understand how hardware operates inside a CPU.
- To know what type of architecture or circuits is suitable in LSI design courses at universities.

Almost 900 single board computers using a KUE-CHIP2 CPU fabricated with commercial ASIC service are used at universities in Japan.

Some lecturers at universities had pointed out weak points of KUE-CHIP2 as follows

- Both memory size for program and for data are limited within 256 bytes.
- Instructions for subroutine call are not supported.

We have redesigned KUECHIP-3F CPU and implement with FPGA to respond to the request [5]. An instruction set architecture of KUECHIP-3F is based on KUE-CHIP2 specification. It is expanded to 16-bit and support Stack Pointer operation instructions like PUSH or POP.

B. Block Diagram

Figure 1 shows a block diagram of KUE-CHIP2 and KUECHIP-3F CPU. They have two data buses: DBi and DBo, an address bus: AB, and an observer bus: OB. Control signals from the outside order the OB to output data of all registers, program counter value, states of flags and memory contents. Users can rewrite contents of registers or a memory directly through the DBi bus. So ROM monitor firmware is not necessary.

There is an Arithmetic/Logic Unit(ALU) and two registers for calculation, an ACCumulator register(ACC) and an IndeX register (IX). A Program Counter(PC) and an Instruction Register(IR) are for instruction fetch. A Memory Address Register(MAR) stores an address from which an instruction or data will be fetched. KUE-CHIP2 and KUECHIP-3F have four kind of flags(FLAG), a zero flag(ZF) , a negative flag(NF), an overflow flag(VF) and a carry flag (CF).

In addition, a Stack Pointer (SP) register is added to KUECHIP-3F.

Buses and registers of KUE-CHIP2 are 8-bit width and of KUECHIP-3F are 16-bit. Accessible memory size of KUE-CHIP2 is 512 bytes: 256 bytes are for program/data and remaining 256 bytes are for data only. KUECHIP-3F can access 65,536 bytes for program/data area. KUE-CHIP2 and KUECHIP-3F can communicate with other computer using the IN and OUT instructions which control IBUF/OBUF ports compliant with Centronics standards.

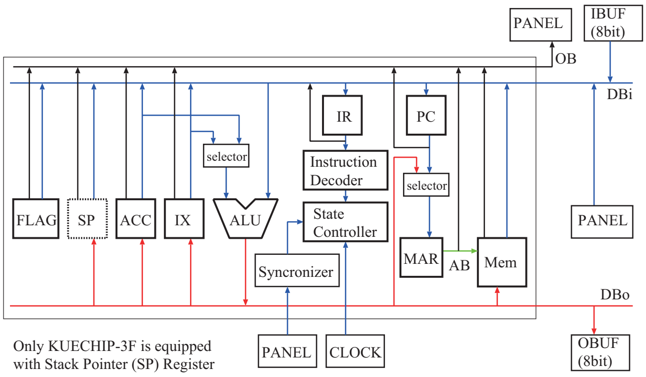

Fig. 1. Block Diagram of KUE-CHIP2 and KUECHIP-3F

C. Instruction set

Table I shows the instruction set of KUE-CHIP2 and KUECHIP-3F. Both CPUs support common 40 instructions: Load/Store, Arithmetic/Logic operation, Shift, Branch, Halt, Set/Reset Carry Flag, INput/OUTput and NOP. In addition KUECHIP-3F supports 6 instructions for Stack Pointer operation. Users of KUECHIP-3F can program subroutine call and return procedure. Both CPU executes an instruction within 3 to 5 clock phases. P0 and P1 are phases for instruction fetch. P2, P3 and P4 phases are for execution.

D. Design for FPGA Implementation

KUE-CHIP2 and KUECHIP-3F CPU are designed with register transfer level (RTL) abstraction using VHSIC hardware description language (VHDL). Xilinx Vivado 2015.4 is used for logic synthesis and mapping to an Artix-7 (XC7A35T) FPGA device. Digilent Nexys-4 DDR Board and Cmod A7 Module are used for verification of the design.

III. RUECHIP2 CPU

A. Outline

RUECHIP2 CPU is designed for an educational material to understand how pipelining processes in typical 5-stage processor architecture. Through programming and observing behavior of RUECHIP2 CPU, a beginner of computer architecture can learn a detail of the pipelining as follows [7].

- Combination of operations in each stage (instruction fetch, instruction decode, execution, memory access and write back) can process instructions collectly
- Data hazards and Control hazards occur in instruction pipeline of CPU
- Forwarding can solve data hazards.

TABLE I
INSTRUCTION SET OF KUE-CHIP2 AND KUECHIP-3F CPU

Load/Store	
LD	LoaD
ST	STore
Arithmetic/Logic Operations	
ADD	ADD
ADC	ADd with Carry
SUB	SUBtract
SBC	SuBtract with Carry
CMP	CoMPare
AND	AND
OR	OR
EOR	Exclusive OR
Shift Operations	
SRA	Shift Right Arithmetically
SLA	Shift Left Arithmetically
SRL	Shift Right Logically
SLL	Shift Left Logically
RRA	Rotate Right Arithmetically
RLA	Rotate Left Arithmetically
RRL	Rotate Right Logically
RLL	Rotate Left Logically
Branch	
BA	Branch Always
BVF	Branch on oVerFlow
BNZ	Branch on Not Zero
BZ	Branch on Zero
BZP	Branch on Zero or Positive
BN	Branch on Negative
BP	Branch on Positive
BZN	Branch on Zero or Negative
BNI	Branch on No Input
BNO	Branch on No Output
BNC	Branch on No Carry
BC	Branch on Carry
BGE	Branch on Greater than or Equal
BLT	Branch on Less Than
BGT	Branch on Greater Than
BLE	Branch on Less than or Equal
Control Program Execution	
HLT	HaLT
SCF	Set Carry Flag
RCF	Reset Carry Flag
IN	INput
OUT	OUTput
NOP	No OPeration
Stack Pointer Operations (only KUECHIP-3F supports)	
INC	INCrement
DEC	DECrement
PSH	PuSH
POP	POP
CAL	CALl
RET	RETurn

B. Block Diagram

Block Diagram of RUECHIP2 CPU is shown in Figure 2. This architecture is based on classic pipeline processing in the textbook: "Computer Organization and Design" by Patterson and Hennessy [6]. The pipelining is composed of 5-stages: Instruction Fetch (IF), Instruction Decode (ID), EX (EXecution), MEM (MEMory access) and WB (Write Back) stage. In the same way as KUE-CHIP2/KUECHIP-3F CPUs, an observer bus (OB) is added to output a value of registers in the pipeline. Followings are register transfer level behavior of RUECHIP2 CPU.

B.1. IF Stage

A Program Counter (PC) holds an address value of an instruction to be fetched next. When it is sent to an Instruction Memory, a fetched instruction will be transferred to an Instruction Register of the IF stage. (if_IR).

B.2. ID Stage

Operation of the ID stage is decoding the fetched instruction of the if_IR register. When the instruction is R-type or I-type, values stored in a register file ($0, $1, ... $31) indicated by Rs and Rt field will be sent to the id_Rs or the id_Rt register. If pipeline register values in the EX, the MEM or the WB stage have been updated by preceding instructions, the Forwarding module will gather values in these stages and writes them to the id_Rs and the id_Rt register. If the instruction is a branch or a jump, a branch condition and a target address for branch/jump will be calculated. When the branch condition is met, the PC in the IF stage will be updated to the branch target.

B.3. EX Stage

If the instruction in the id_IR register is Arithmetic/Logic/Shift operations, the calculated result by the ALU is stored in the ex_C register. If the instruction is Load or Store, the memory address to be accessed is calculated and stored in the ex_C register. If the instruction is Store, the data to be stored in a data memory is transferred to the SMD register.

B.4. Mem Stage

In this stage the CPU will access to the data memory if an instruction in an ex_IR register is Load or Store. If it is Load, data returned from the data memory will be placed in a mem_C register. In case of Store instruction, data in the SMD register will be transferred to the data memory addressed by the ex_C register.

B.5. WB Stage

When an instruction of a mem_IR register is R-type or I-type, in this stage the CPU writes the calculation result in a mem_C register to one of the register file which is indicated by Rd (R-type) or Rt (I-type) field. If the instruction is Load, data from the data memory in the mem_C register is transferred to the register file.

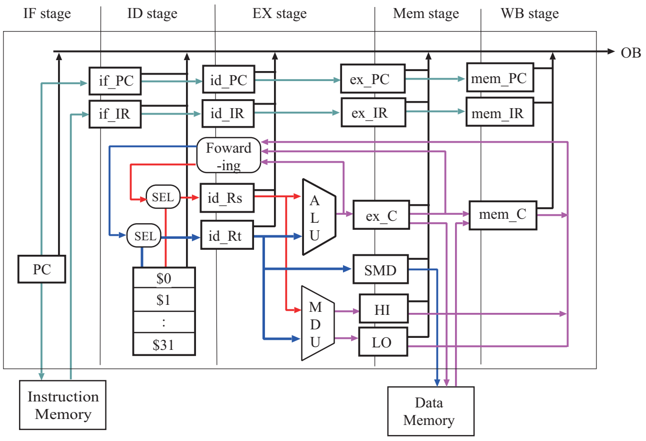

Fig. 2. Block Diagram of RUECHIP2

C. *Instruction Set*

The instruction set of RUECHIP2 CPU is shown in Table II. Except for instructions for Floating Point Unit (FPU) and Memory Management Unit (MMU), all instructions of MIPS R3000 are implemented. Binary codes generated by the GNU C Compiler invoked with R3000 architecture option can be executed by RUECHIP2 CPU. If a RUECHIP2 user wants to do floating point calculations, soft-float emulation library for GCC should be compiled and linked together[8].

D. *Logic Design for FPGA*

RTL design of RUECHIP2 CPU is done using Verilog hardware description language (Verilog-HDL). As with the design of KUE-CHIP2 and KUECHIP-3F CPUs, Xilinx Vivado 2015.4 is used for logic synthesis and mapping to an Artix-7 (XC7A35T) FPGA device. Cmod A7 Module is used for verification of the design.

IV. KR-Chip and Single Board Computer

A. *Block Diagram*

Block Diagram of KR-CHIP is shown in Figure 3. 3 CPUs : KUE-CHIP2, KUECHIP-3F and RUECHIP2 are integrated in an Artix-7 (XC7A35T) FPGA. Main memory for KUE-CHIP2 and KUECHIP-3F is a Block RAM generated by the Block Memory Generator of Xilinx Vivado 2015.4. RUECHIP2 CPU uses an On Board SRAM

TABLE II
Instruction set of RUECHIP2 CPU

Load/Store	
LB	Load Byte
LBU	Load Byte Unsigned
LH	Load Halfword
LBU	Load Halfword Unsigned
LW	Load Word
LWL	Load Word Left
LWR	Load Word Right
SB	Store Byte
SH	Store Half Word
SW	Store Word
SWL	Store Word Left
SWR	Store Word Right
Arithmetic/Logic Operations	
ADD	ADD
ADDU	ADD Unsigned
SUB	SUBtract
SUBU	SUBtract Unsigned
SLT	Set Less Than
SLTU	Set Less Than Unsigned
AND	AND
OR	OR
XOR	eXclusive OR
NOR	NOR
ADDI	ADD Immediate
ADDIU	ADD Immediate Unsigned
SLTI	Set Less Than Immediate
SLTIU	Set Less Than Immediate Unsigned
ANDI	AND Immediate
ORI	OR Immediate
XORI	eXclusive OR Immediate
LUI	Load Upper Immediate
Shift Operations	
SLL	Shift Left Logical
SRL	Shift Right Logical
SRA	Shift Right Arithmetic
SLLV	Shift Left Logical Variable
SRLV	Shift Right Logical Variable
SRA	Shift Right Arithmetic Variable
Multiple/Divide Operations	
MULT	MULTiply
MULTU	MULTiply Unsigned
DIV	DIVide
DIVU	DIVide Unsigned
MFHI	Move From HI
MTHI	Move To HI
MFLO	Move From LO
MTLO	Move To LO
Branch	
	Branch
BEQ	on EQual
BNE	on Not Equal
BLEZ	on Less than or Equal to Zero
BLTZ	on Less Than Zero
BGEZ	on Greater than or Equal to Zero
BLTZAL	on Less Than Zero And Link
BGEZAL	on Greater than or Equal to Zero And Link
Jump	
J	Jump
JR	Jump Register
JAL	Jump And Link
JALR	Jump And Link Register
System Control Coprocessor CP0 Instructions	
MTC0	Move To Cp0
MFC0	Move From Cp0
RFE	Return From Exception
Special Instructions	
STSCALL	System CALL
BREAK	BREAK

(512kB) for program and data memory. Instruction fetch and data access to the On Board SRAM by RUECHIP2 CPU is controlled by the memory controller through an AXI Interconnect. A Serial Peripheral Interface (SPI) IP and a Block RAM (2port) are connected to slave interfaces of the AXI Interconnect. Digilent Pmod modules which are compliant with the SPI standard can be added. A user of RUECHIP2 CPU can perform high speed external communication through the SPI IP. When Digilent Pmod modules which do not correspond to the SPI standard are needed, User-Logics for between a Block RAM (2port) and the Pmod modules should be implemented.

Every CPU in the KR-CHIP can be controlled by commands from the Micro controller or RS232C Serial Interface of the Personal Computer (PC). The control commands defined for KR-CHIP are as follows.

- Write Program/Data in the main memory of each CPU
- Start or Stop Program Execution
- Observe a value of the internal register of each CPU

The Terminalbox Module interprets the commands sent from the outside and does the defined control above mentioned. The Terminalbox Module is tightly coupled with 3 CPUs and can control the program execution of each CPU as follows.

- Execute one instruction or one clock phase of instruction
- Change program execution speed continuously while running, from 10 MHz to 0.1 Hz

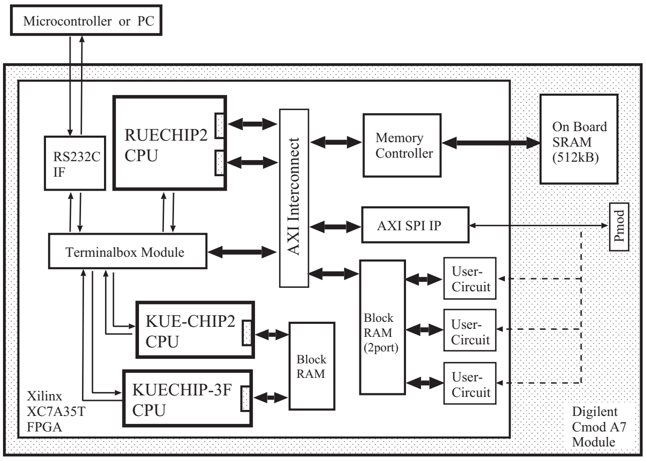

Fig. 3. Block Diagram of KR-CHIP

B. FPGA Implementation of KR-CHIP

KR-CHIP equipped with KUE-CHIP2, KUECHP-3F and RUECHIP2 CPU is synthesized with Xilinx Vivado 2015.4 and mapped to a Xilinx Artix-7 FPGA device on Digilent Cmod A7 module. Table III summarizes the result of synthesis and mapping result of KR-CHIP. Subcolumns "LUTs", "FF" and "delay [ns]" show the number of the look-up tables, the number of the flip-flops and the critical path delay.

TABLE III
FPGA Mapping Result

LUT	FF	delay [ns]
16,687 (80.2%)	12,175 (29.3%)	40.7

C. Single Board Computer for Education

A single board computer for education using KR-CHIP has been developed. Figure 4 shows the top view of this board. KR-CHIP is implemented in a Xilinx Aritx-7 FPGA of a Digilent Cmod A7 module. A user can program one of KUE-CHIP2, KUECHIP-3F or RUECHIP2 CPU and observe how instructions are executed in it.

Which CPU to be programmed can be selected by a toggle switch or a slide switch on the board. When KUE-CHIP2 or KUECHIP-3F is selected, these three buttons control program execution as follows.

- SP : Execute one clock phase of instuction execution and halt
- SI : Execute one instruction and halt
- SS : Start program execution when it is stopped. Stop program execution when it is running.

When RUECHIP2 is selected,

- SP : Execute one clock phase of instuction execution and halt
- SS : Start program execution when it is stopped. Stop program execution when it is running.

This single board computer has a Vacuum Fluorescent Display(VFD) which shows 4 lines with 20 alphanumeric characters. This VFD shows

- Selected CPU is running or halt
- 8/16/32-bit value entered on a hexadecimal keyboard
- Register value of selected CPU in KR-CHIP
- Memory address and its contents (instruction or data)

Values can be displayed in hexadecimal or disassembled instruction of each CPU.

Three communication ports, four expansion connectors and three SMA connectors are prepared as follows.

- Communication ports (CN1 and CN2) for communication experiment between two KR-CHIP boards
- RS232C serial communication ports (CN3) for transferring assembled binary codes from PC to the main memory of each CPU.

- Four Pmod connectors (Pmod_1 ∼ Pmod_4) for Digilent Pmod Modules
- Three SMA connectors (SMA_1 ∼ SMA_3) for power dissipation measurement of each CPU core by a digital oscilloscope. It can be used to evaluate tamper resistance of cryptographic software or circuits when it is attacked in non-invasive way called side-channel attacks[9].

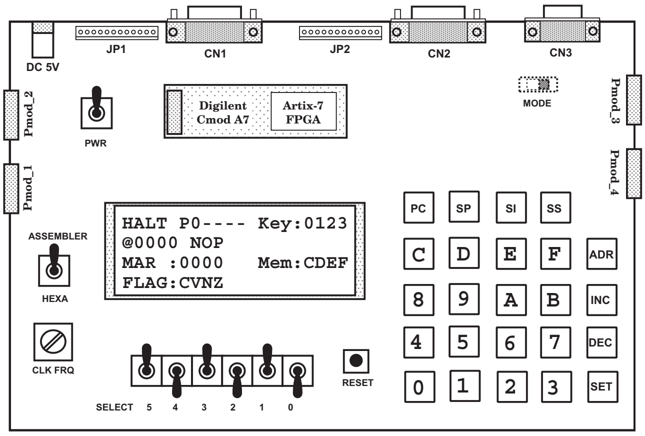

Fig. 4. Top view of KR-CHIP Single Board for Education

V. Summary

We have developed KR-CHIP for computer education which consists of 3 CPUs: KUE-CHIP2, KUECHIP-3F and RUECHIP2. KUE-CHIP2 CPU is 8-bit accumulator-based and KUECHIP-3F CPU is 16-bit accumulator-based architecture with simple instruction set. RUECHIP2 CPU is based on 32-bit 5-stage classic pipeline introduced by the text book by Patterson and Hennessy. These 3 CPUs in the KR-CHIP have features that a user can observe how instructions are processed in these CPU cores. Data of all registers, counters or data/address bus in the CPUs can be displayed in hexadecimal or in disassembled instruction using a KR-CHIP single board computer. Also program execution can be suspended and restarted at any cycle or at any clock phase. This single board for education has been used at Ritsumeikan Univ. since 2018. We believe that this system is useful for beginners of the computer architecture to grasp a physical image of a CPU hardware.

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References

[1] H. Kanbara: "KUE-CHIP: A Microprocessor for Education of Computer Architecture and LSI Design," in Proc. IFIP Workshop on Design and Test of ASICs, pp.15-18(1990).

[2] H. Ochi, H. Sawada, K. Okada, A. Uejima, H. Kanbara, K. Hamaguchi and H. Yasuura: "A Microprocessor for Education of Computer Engineering and integrated Circuit Design:KUE-CHIP2 (in Japanese)," IPSJ SIG Technical Reports 1992-ARC-96-13(1992).

[3] H. Kanbara, H. Ochi, H. Sawada, H. Hamaguchi, K. Okada, A. Uejima and H. Yasuura: "KUE-CHIP2 Design Document(in Japanese)," ASTEM RI(1992).

[4] H. Kanbara, H. Ochi, H. Sawada, H. Hamaguchi, K. Okada, A. Uejima and H. Yasuura: "KUE-CHIP2 Education Board Reference Manual(in Japanese)," ASTEM RI(1992).

[5] K. Azuma, Y. Oosako, A. Shibata, H. Kanbara and Y. Kunieda: "Development of a 16bit Microprocessor for Education: KUECHIP-3F(in Japanese)," in Proc. Convention of IPSJ Kansai Section, A-04(Sept. 2017).

[6] David A. Patterson and John L. Hennessy: "Computer Organization and Design - 5th Edition," Morgan Kaufmann(2013).

[7] H. Kanbara, R. Kinjo, Y. Toda, M. Yano and S. Oyanagi: "RUECHIP1 Processor: Teaching Material for Understanding a Pipeline Processor(in Japanese)," in Proc. Convention of IPSJ Kansai Section, A-9(Sept. 2009).

[8] H. Takebayashi, N. Ito, S. Tamura H. Kanbara, and N. Ishiura: "FPGA Simulation of Motor in Floating Point Precision Using Binary Synthesizers ACAP(in Japanese)," in Proc. Convention of IPSJ Kansai Section, A-02(Sept. 2014).

[9] H. Kanbara, N. Ito, H.Takebayashi, M. Takenae, and T.Tsukamoto: "FPGA Prototyping of a Smart Card Platform for Evaluating Tamper Resistance of Cryptographic Circuits," Proc. Workshop on Synthesis And System Integration of Mixed Information Technologies (SASIMI 2016), R1-14 (2016).