NR-Router: A Network-Flow-Based Routing Algorithm for Electrowetting-on-Dielectric Microfluidics with Non-Regular Shape Electrodes

Hsin-Chuan Huang, Tsung-Yi Ho
Department of Computer Science, National Tsing Hua University, Hsinchu, Taiwan

***Abstract*—Due to the advances in microfluidics, electrowetting-on-dielectric (EWOD) chips have been widely applied to various laboratory procedures. To ease the process of designing EWOD chips, the prototype of a cloud-based open-source EWOD cyber manufacturing ecosystem has been proposed [1]. This ecosystem introduces the non-regular shape electrodes and glass-based chips to provide multi-functional and high-reliability EWOD chips, which can achieve more complex operations (e.g., different-size droplets control, precise droplet movement). None of the existed work, however, considers the routing for glass-based EWOD chips with non-regular shape electrodes, which hinders the implementation and development of this ecosystem since users are burdened with time-consuming wire connections. Unlike regular shape electrodes, routing resource manipulation and pin access of non-regular shape electrodes further complex the routing problem. In this paper, we propose a network-flow-based routing algorithm called NR-Router that can correctly route in glass-based EWOD chips with non-regular shape electrodes for the first time. We construct a minimum cost flow problem to generate optimal routing paths followed by a light-weight model to reduce the run time. NR-Router achieves 100% routability while minimizing wirelength at a low run time and can generate mask files that can be directly put into manufacturing. Experimental results show the robustness and efficiency of the proposed algorithm.**

I. Introduction

Electrowetting-on-dielectric (EWOD) chips have been appreciated as a promising actuator for digital microfluidic (DMF) systems [2]. EWOD chips can reduce both sample consumption and experimental time drastically, and make continuous sampling and analysis possible for real-time biochemical analysis. Tiny droplets through the electrowetting in a "digital" manner under clock control can be manipulated on a 2-D array of electrodes.

Although EWOD chips have attracted significant attention, the development of EWOD chips suffers from two main bottlenecks: technical barriers and reliability issues [1], as shown in Fig. 1. Technical barriers refer to the manufacturing of EWOD chips, which requires specific facilities, professional knowledge, and the building of control electronics and software to operate EWOD chips. Reliability issues refer to the primary failure mechanisms of the chips during usages, such as the current leakage (short-term failure often manifested as electrolysis) through the dielectric layer, and the electric charging (long-term degradation often stalling the electrowetting effect) of the hydrophobic topcoat on the EWOD chip.

To ease the process of designing and eliminate the burden of fabricating EWOD chips, the prototype of a cloud-based open-source EWOD cyber-manufacturing ecosystem has been proposed [1]. This ecosystem introduces the non-regular shape electrodes and glass-based chips to provide multi-functional and high-reliability EWOD chips, which can achieve more complex operations (e.g., different-size droplets control, precise droplet movement). The EWOD chips with non-regular shape electrodes can effectively reduce the difficulty of biochemical experiments designing (easier to design the chip that meets the experiment). In this ecosystem, users can design the architecture of EWOD chips online using electrodes with various shapes without considering the burden of manufacture, and share chip designs, which helps biochemists overcome the technical barriers of designing customized EWOD chips for experiments.

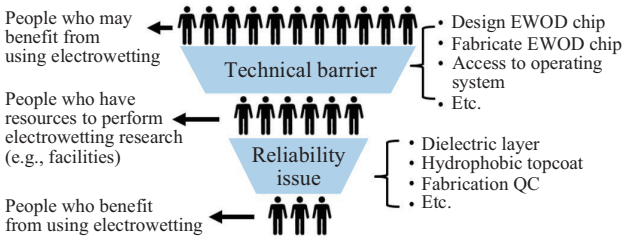

Fig. 1. Technical barrier and reliability issues are two major bottlenecks that limit the growth of electrowetting community [1].

However, there is a serious problem that hinders the implementation and development of the ecosystem. None of the existed work considers the routing for glass-based EWOD chips with non-regular shape electrodes. This results in users are burdened with time-consuming wire connections, namely, must manually route the wires from the electrodes to the contact pads (external control circuit). Thus, automatic routing tools for glass-based EWOD chips with non-regular shape electrodes are indispensable.

Most existing approaches focus on a printed circuit board (PCB)-based EWOD chips [3], [5] and paper-based EWOD chips [4]. In PCB-based EWOD chips, the bottom plate contains a patterned array of individually controlled electrodes. The top plate is coated with a continuous ground electrode [3], [6], as shown in Fig. 2(a). The wires can be routed from the pin to the electrical pad without considering the obstacles by electrodes. Since [3], [5] did not consider the obstacles incurred by electrodes, previous methods cannot route the wires for glass-based EWOD chips.

On paper-based EWOD chips, electrodes and wires should be placed in the same layer, as shown in Fig. 2(b). Wang et

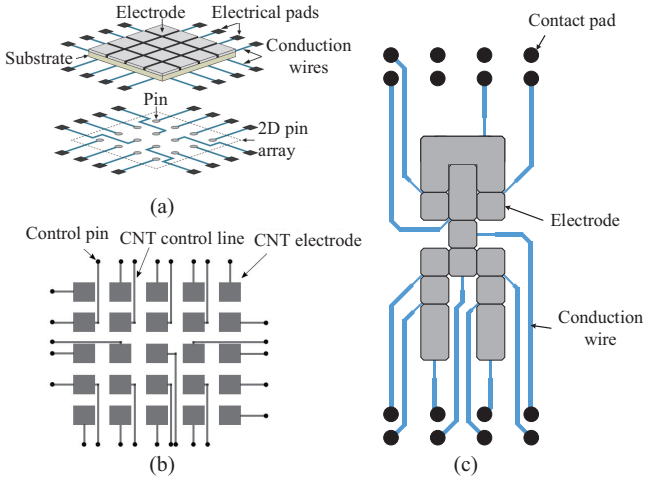

Fig. 2. (a) Routing on PCB-based EWOD chips [3]. (b) Routing on paper-based EWOD chips [4]. (c) Routing on [1] dedicated EWOD chips.

al. [4] proposed the minimum cost flow formulation based on routing grids. However, the routing algorithm for paper-based EWOD chips cannot be adapted for glass-based EWOD chips for the following reasons: 1). In order to avoid printed ink pollution on the paper-based EWOD chip, it requires larger space between electrodes than glass-based EWOD chip; 2). The wires of paper-based EWOD chips should be routed with 90° on every turn. On the contrary, the wires of glass-based EWOD chips can be routed with 45° on each turn, which effectively circumvents the issue of acid traps. Furthermore, to conduct general experiments, non-regular shape electrodes are introduced. As a result, previous routing algorithms cannot be applied to glass-based EWOD chips with non-regular shape electrodes, as shown in Fig. 2(c). Unlike regular shape electrodes in the PCB-based or paper-based EWOD chip, routing resource manipulation and pin access of non-regular shape electrodes in a glass-based EWOD chip further complex the routing problem.

To fundamentally solve the problems above, in this paper, we propose NR-Router, a network-flow-based routing algorithm that can correctly route in glass-based EWOD chips with non-regular shape electrodes for the first time. Our contributions include:

- We propose an algorithm that can effectively resolve the routing problem on glass-based EWOD chips with non-regular shape electrodes while minimizing the total wirelength.
- We adopt an effective pin selection method based on the minimum cost network-flow formulation, which routes wires from electrodes to contact pads with optimal connection pins to achieve ideal routing results. Besides, we propose a light-weight model to reduce the run time of the minimum cost flow problem.
- We solve a severe problem faced by the implementation and development of a promising ecosystem. In addition, the design and application of the EWOD chip are advanced since the automatic routing tools of EWOD with non-regular shape electrodes become feasible.
- We evaluate the proposed method using three synthetic benchmarks and a biochemical application. Experimental results show the robustness and efficiency of our algorithm. Our algorithm achieves 100% routability while minimizing wirelength at a low run time, and can generate mask files that can be directly put into manufacturing.

The paper is organized as follows. Section II describes the architecture of electrodes and problem formulation. Section III introduces the pin selection of non-regular shape electrodes. Section IV introduces the details of NR-Router. Experimental results are reported in Section V. Section VI introduces the automatic mask generation, and we conclude this paper in Section VII.

II. The Architecture of Electrodes and Problem Formulation

In this section, we first introduce the architecture of the electrodes. Then, we introduce the electrodes merging procedure for enhancing the reliability of the biological experiment. Finally, we define the problem formulation of this paper.

A. Architecture of the Electrodes

In [1], the base electrodes are designed in an octagonal shape with a connection pin on each edge to utilize the routing area efficiently. To ensure the wire can route from the corner between the gap of adjacent electrodes, the width of wires contacting electrodes is half. Based on the actuation mechanism of EWOD, droplets are moved by applying a control voltage to an electrode adjacent to the droplet and, at the same time, deactivating the electrode just under the droplet. In order to avoid the voltage influence between electrodes and conduction wires, there are spacing constraints that the conduction wires and electrodes should not be placed over closely.

B. Electrodes Merging

To ensure the stability of the biological experiment, researchers usually require electrodes with various shapes to apply to several functions (e.g., control droplets of different sizes, move droplets precisely). Besides, reagents with different volume would be transported through electrodes with different shapes. The reliability of biological experiments can be promoted via assembling various electrodes. The number of connection pins in each electrode is determined by the shape of electrodes when any electrodes merge. By [1], users can merge multiple base electrodes into a large electrode with various shapes, handling many specific functions (e.g., waste pool path, direction reservoir, and long electrode).

C. Problem Formulation

To drive these electrodes by assigning time-varying actuation voltage, we need to connect conduction wires between electrodes and contact pads (external control circuits). This routing problem can be formulated as follows:

- ***Input:*** The locations of contact pads and electrodes, the shape of electrodes, and chip specification.
- ***Output:*** The routing paths between electrodes and contact pads.
- ***Objective:*** Maximize the routability of routing result, while minimizing the total wirelength.

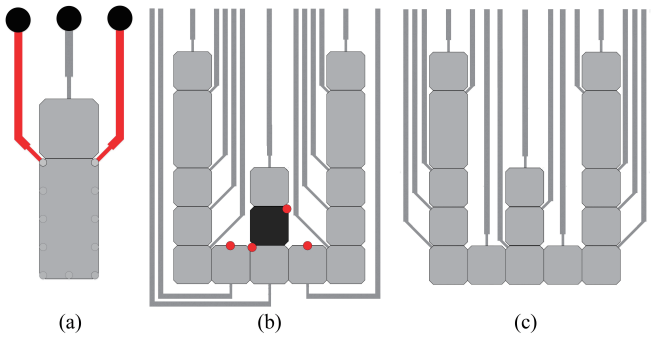

Fig. 3. (a) Multiple pins that are close to contact pads. (b) The routing situation cannot achieve 100% routability. (c) The routing situation achieves 100% routability while minimizing wirelength.

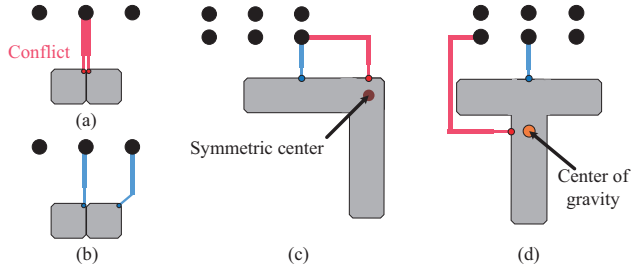

Fig. 4. (a) Conflict happens. (b) Appropriate selection of candidate pins considering all candidate pins. (c), (d) Detour happens when center of gravity or symmetric center is chosen.

III. Pin Selection of Non-Regular Shape Electrodes

In this section, we first explain the importance of candidate pin selection. Then, we focus on the candidate pin selection of non-regular shape electrodes.

A. Candidate Pin Selection

There are many connection pins in an electrode that can be chosen to route the wire. If a connection pin is chosen, we call the connection pin as a *Candidate Pin*. The selection of candidate pin may influence not only the routability but also the wirelength. The naive way to select a candidate pin is to choose the pin closest to contact pads. Nevertheless, sometimes there are multiple pins closest to contact pads, as shown in Fig. 3(a). If we select the inappropriate candidate pin, an infeasible routing result may happen. For example, Fig. 3(b) shows that the red pins cannot route from the electrodes because other wires occupy the routing area. Fig. 3(c) shows the appropriate candidate pins selection and the ideal routing result with shorter wirelength. Consequently, an appropriate selection of candidate pins is essential.

Selection of candidate pins must consider all selections of candidate pins of each electrode simultaneously, or the routing result will not be ideal. For example, two electrodes can be connected to the contact pad with the minimal wirelength, but the contact pad can only be connected to one of them. In this situation, the conflict will happen and lead to an infeasible routing result. Fig. 4(a) shows that the conflict happens when both electrodes are connected to the closest to the contact pad. Fig. 4(b) shows the better selection of candidate pins considering all candidate pins of other electrodes simultaneously.

B. Non-Regular Shape Electrode

The number of connection pins of non-regular shape electrodes varies, which complexes the problem to select the candidate pins. In a non-regular shape electrode, the option of candidate pin becomes numerous as long as more electrode units merging. We cannot determine the appropriate candidate pin quickly. If the pin closest to the symmetric center or center of gravity of the non-regular shape electrode by the light of nature is chosen, a detour might happen, as shown in Fig. 4(c)(d). Since the manufacturing cost increases as the wirelength increases, we should select the appropriate candidate pin with the shortest routing path and consider all selections of candidate pins of each electrode simultaneously. As a result, the selection of candidate pins becomes much more difficult in non-regular shape electrodes.

IV. Details of the Proposed Method

In this section, we propose NR-Router, a network-flow-based routing algorithm. We first give the overall of the proposed routing algorithm. Then, we introduce the pseudo node and show how to construct the corresponding minimum cost flow problem. Finally, we show the light-weight model, which reduces the run time of the minimum cost flow problem.

A. Overall Algorithm

We construct a minimum cost flow problem of routing followed by a light-weight model. In the minimum cost flow problem, we first consider a non-regular shape electrode as an electrode pad composed of multiple electrode units and apply a pseudo node to connect each electrode unit in each electrode pad, and then adopt the network-flow approach to generate optimal routing paths. In the light-weight model, we control ingoing flow and outgoing flow via the two-layers tile to reduce the redundant calculations for routing in [1].

Fig. 6 summarizes the overall flow of NR-Router. In flow graph construction, each tile and each grid is respectively represented by a tile node and a grid node. The pseudo nodes are added for each electrode pad. In applying the network-flow algorithm, we construct the minimum cost flow formulation, which contains all connected edges and cost among tile nodes, grid nodes, electrode pads, and contact pads according to the connectivity in the mesh. The distance in the real world between every two nodes determines the cost of the edges between tiles and grids. In the flow collocation procedure, a pairing algorithm is applied to prevent wire overlapping.

B. Pseudo Node and Minimum Cost Flow

Although [4], [7] proposed the minimum cost flow formulation based on routing grids, these methods cannot be applied to EWOD chips with non-regular shape electrodes. Thus, we propose the minimum cost flow formulation for the routing algorithm and obtain the appropriate selection of candidate pins. According to the width of the electrode unit, the routing area can be partitioned into a mesh by horizontal and vertical lines with uniform spacing. *Tiles* are formed by two adjacent horizontal lines and two adjacent vertical lines, and *Grids* are the intersection points between these horizontal and vertical lines. We consider a non-regular shape electrode

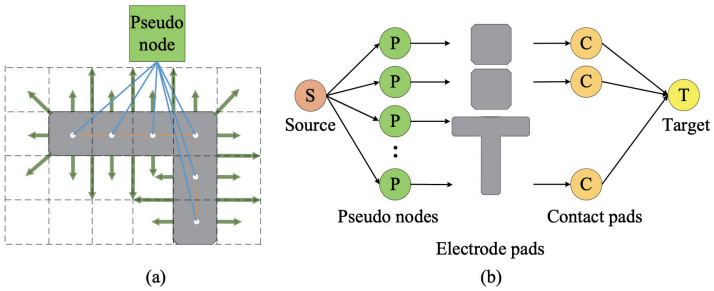

Fig. 5. (a) The pseudo node structure. (b) The schematic diagram of the flow direction in our network-flow algorithm.

as an *Electrode Pad* composed of multiple *Electrode Units* and introduce the *Pseudo Node* structure base on the network-flow model, as shown in Fig. 5(a). As choosing candidate pins before routing is challenging, we consider all connection pins as the feasible routing paths. Fig. 5(b) shows the network-flow graph $G = (V, E)$ where each edge $(u, v) \in E$ has capacity $c(u, v)$, flow $f(u, v)$ and cost $a(u, v)$. The corresponding minimum cost flow problem is constructed as follows:

- A super source node S and super target node T are added into V, with capacity ∞ and unit flow cost 0.
- For each pseudo node in P and contact pad in C, a node p_i and c_j is added into V, with capacity 1 and unit flow cost 0.
- For each electrode unit, a node is added into V, with capacity 1 and unit flow cost 0.
- For each grid that is not covered by electrodes or contact pads, a node is added into V, with capacity 1 and unit flow cost 0.
- For each tile that is not covered by electrodes or contact pads, a node is added into V, with capacity γ and unit flow cost 0. The γ depends on the wire width.
- A directed edge is added into E for each (S, p_i), (c_j, T), between the pseudo nodes and electrode units in each electrode pad, between the electrode units and tiles, and between the electrode units and grids according to the connectivity in the mesh, with capacity 1 and unit flow cost 0.
- A bi-directional edge is added into E between each pair of grids or tiles, with capacity 1 and unit flow cost 1.
- **Objective**: Minimize $\sum_{(u,v)\in E} a(u, v) \cdot f(u, v)$

C. Light-Weight Model

In the traditional network-flow model [8], [9], tile nodes are introduced to represent a tile. The number of wires that can pass through a tile is called flow capacity. Flow capacity usually categorized into *Orthogonal Capacity* (O-cap) and *Diagonal Capacity* (D-cap), as shown in Fig. 7(a). Most of the previous network-flow models only concern the O-cap. In these models, edges are added from tile nodes to either adjacent tile nodes or pin nodes. However, diagonal capacity D-cap is not mentioned by these models. For example, consider the case that O-cap = 2 and D-cap = 3, as shown in Fig. 7(b)(c). These models cannot capture the number of wires passing through the diagonals of the tile. The model proposed by [7] can handle all situations and capture the correct O-cap and D-cap, as shown in Fig. 8. However, there are 5 tile nodes and 16 edges inside a

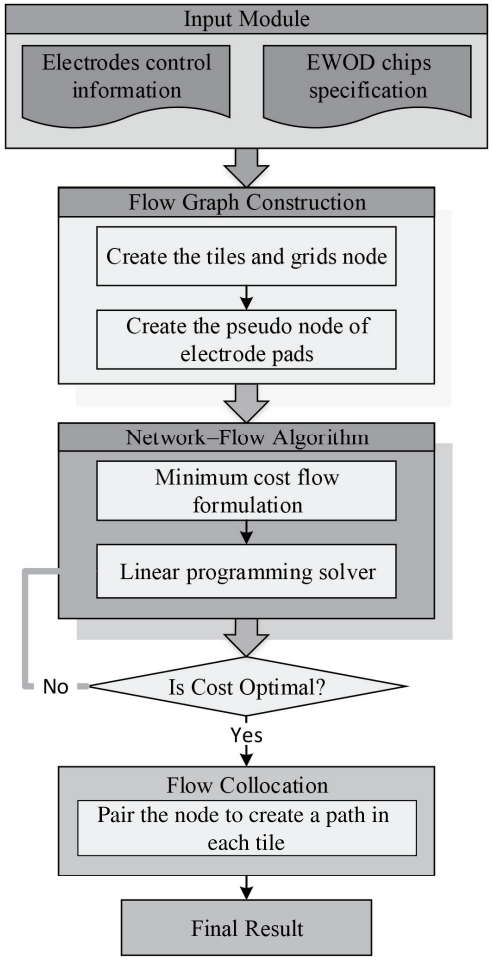

Fig. 6. Flow chart of NR-Router.

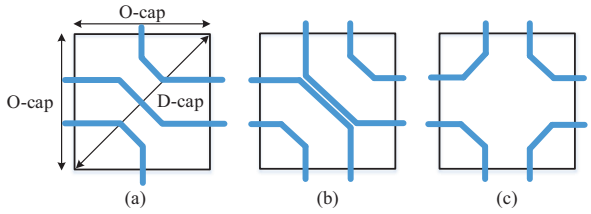

Fig. 7. An example of routing problem in a tile. (a) *O-cap*=2 and *D-cap*=3. (b) [8] may lead to illegal routing. (c) [9] cannot catch the logical routing.

tile, which are more than the traditional network-flow model. In [1], the contact pads are located on the upper and lower side of the chip. Therefore, the routing flows must be upward or downward, as shown in Fig. 9. Due to the restriction of flow direction, the model proposed by [7] produced extensive redundant calculations for routing in [1].

We propose a light-weight model that can handle the O-cap and D-cap correctly. This model considers a tile as two layers, and one layer mainly controls the ingoing flow, and the other controls the outgoing flow. Note that ingoing flow and outgoing flow represent the flow goes into or out of the tile. Each layer is represented by a tile node and adding four directed edges between adjacent tile nodes. For every two tile nodes in a tile, a directed edge is added between two layers as D-cap and

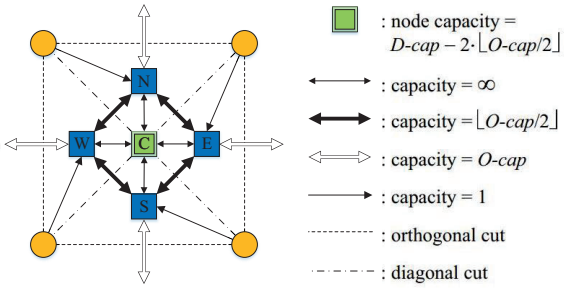

Fig. 8. The model proposed by [7] inside a tile.

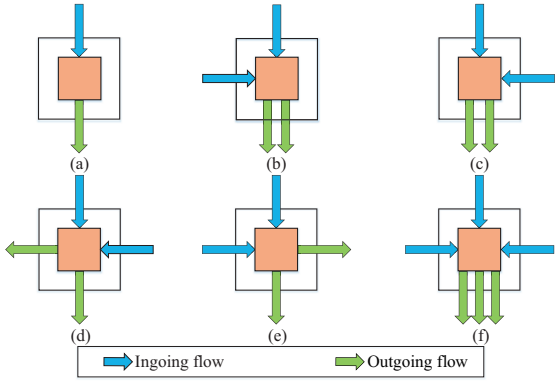

Fig. 9. The downward flows inside a tile.

with cost 0. The directed edge between two layers can prevent the total passed flow from exceeding the capacity of the tile. Since the contact pads are located on the side of chips in [1], upward and downward flows cannot exist simultaneously. The downward flows are shown in Fig. 9. The blue arrows denote the ingoing flows, and the green arrows denote the outgoing flows. The upward flows are directed in the opposite of Fig. 9. With the proposed model, we can achieve the same routability and reduce memory usage and time consumption.

D. Flow Collocation in a Tile

The wires should not overlap with each other. Otherwise, the voltage will affect each other. As a result, the flow control is an essential issue in network-flow algorithm. In order to prevent the flows from crossing over, flow collocation is introduced. First, label the angles of ingoing flows in ascending order and the angles of outgoing flows in descending order (upper left corner is $0°$ reference point). Afterwards, we pair the flows in order. For example, in Fig. 10(b), the ingoing flow F_1 with the minimal angle θ_1 will be paired with the outgoing flow F_6 with the maximal angle θ_6. Follow by the similar rule, (F_2, F_5) and (F_3, F_4) are paired respectively. As a result, we can avoid crossings between wires in a tile.

V. Experimental Results

NR-Router was implemented in Python and tested on a PC with 3.4 GHz CPU and 24GB memory. We used the minimum cost flow solver OR-Tools [10] to obtain the minimum cost flow solution of our network-flow model.

We first introduce the model proposed by [7] and our light-weight model into NR-Router respectively. Although the

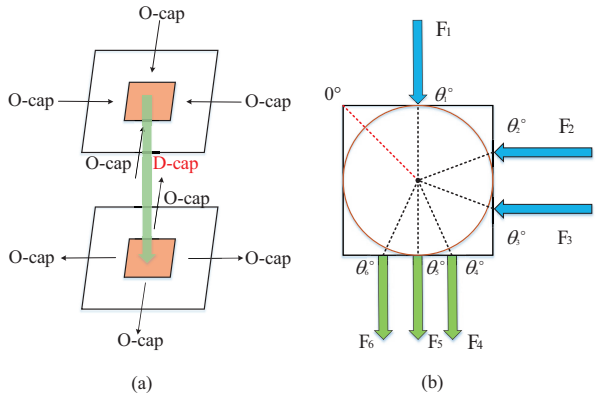

Fig. 10. (a) The light-weight model. (b) The flow collocation in a tile, and the angle increases in a clockwise direction.

model proposed by [7] can obtain the same 100% routability with our light-weight model, redundant calculations for routing are produced. Fig. 11 shows the comparison of the run time. For the same benchmark, our light-weight model obtained a shorter run time and a lower time growth rate on the large scale of the benchmark.

Then, we used four benchmarks to verify NR-Router. The dilution function EWOD chip is a real-life biochemical application from [1], and the other three are synthetic benchmarks. For comparison, we implemented the exhaustive network-flow algorithm and the A* algorithm, that can route in glass-based EWOD chips with non-regular shape electrodes. In the exhaustive network-flow algorithm, wires are routed after the candidate pins are determined, and all combinations of candidate pins between each electrode will be computed. We denote the number of pins in each electrode as $P_{E_{es}}$, and all possible combinations will reach up to $\prod_{k=1}^{n} P_{E_k}$, where P_{E_k} denotes the number of connection pins in electrode E_k. In the A* algorithm, each electrode is connected to the closest contact pad in sequence.

Table I shows the experimental results. The number of electrodes is shown in column N_E. As shown in the table, all algorithms achieved 100% routability in each case. NR-Router performed optimal wirelength and reduced CPU time significantly. The exhaustive network-flow algorithm, which tried all possible combinations of candidate pins, consumes significant time even with the smallest benchmark. Although the A* algorithm had excellent efficiency in the shortest path problem, the optimal wirelength cannot be obtained. In the case of a large number of electrodes, the CPU time of A* algorithm did not scale well because of the increasing computation complexity while paths were decided.

Ultimately, our experimental results had proved the robustness and scalability of NR-Router. In all cases, the optimal wirelength and surprisingly CPU time were obtained even if the number of electrodes increased. Fig. 12 shows the routing solution of the real-life dilution function EWOD chip.

VI. Mask Generation

For glass-based EWOD chips, the fabrication file is in DXF. The mask file required for chip fabrication is usually generated manually, which is very time-consuming. Thus, we generate

TABLE I
WIRELENGTH AND CPU TIME OF NR-ROUTER AND TWO BASELINE SOLUTIONS

Benchmark	Number of Electrode Pads (N_E)	Exhaustive Algorithm		A* Algorithm		NR-Router	
		Wirelength (um)	CPU Time (s)	Wirelength (um)	CPU Time (s)	Wirelength (um)	CPU Time (s)
Test_case1	5	98798	>1 hour	125971	0.2284	98798	0.2024
Test_case2	7	132175	>1 hour	186293	0.5572	132175	0.2089
Test_case3	10	178208	>1 hour	264026	0.6716	178208	0.1994
Dilution Function EWOD chip	100	2243131	>1 hour	3418597	2.0769	2243131	0.3674

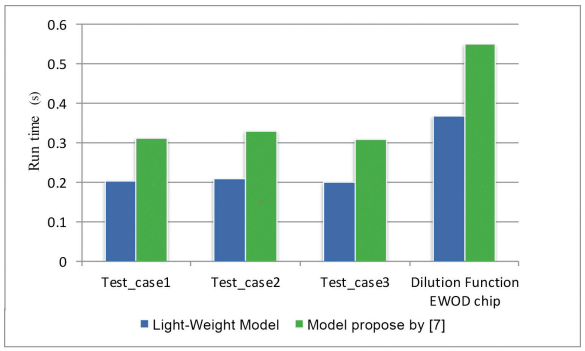

Fig. 11. The light-weight model compared with the model proposed by [7].

the mask file automatically in routing automation. Due to the width of the corner with a 45° angle is different from the width of a straight wire, the generated masks are infeasible when we draw the rectangle to connect the corners, as the notch shown in Fig. 12(a). We need to calculate the coordinates and draw a quadrilateral instead of a rectangle. As shown in Fig. 12(b), the referenced node coordinates are determined by the connections of paths.

VII. CONCLUSIONS

In this paper, we have proposed NR-Router, a network-flow-based routing algorithm that can correctly route in glass-based EWOD chips with non-regular shape electrodes for the first time. NR-Router effectively solves the pin access and routing problem while considering all connection pins of electrodes simultaneously and comprehensively, and can generate mask files that can be directly put into manufacturing. The proposed light-weight model reduces the run time of the minimum cost flow problem. Besides, the design and application of the EWOD chip are advanced since the automatic routing tools of EWOD with non-regular shape electrodes become feasible. Experimental results on real-life chip application and test designs have demonstrated the robustness and efficiency of our algorithm.

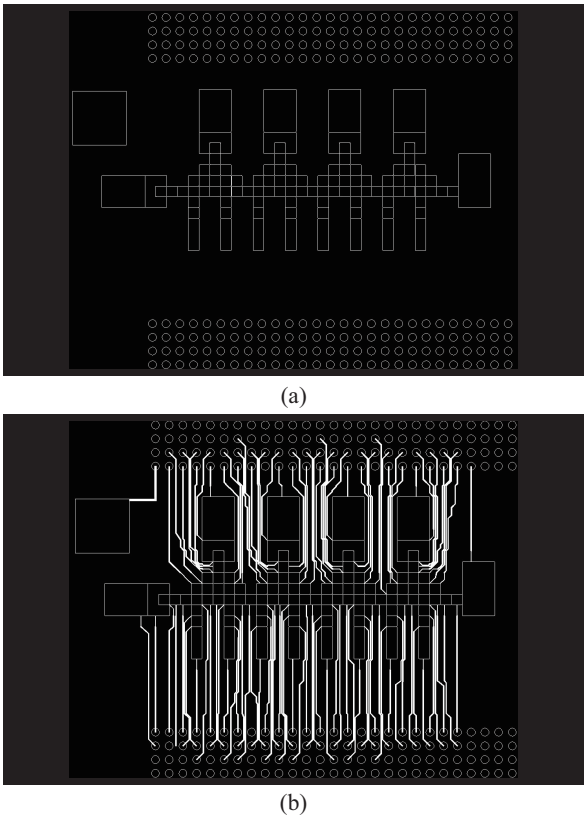

Fig. 12. (a) The architecture of EWOD chip. (b) The routing result of dilution function EWOD chip.

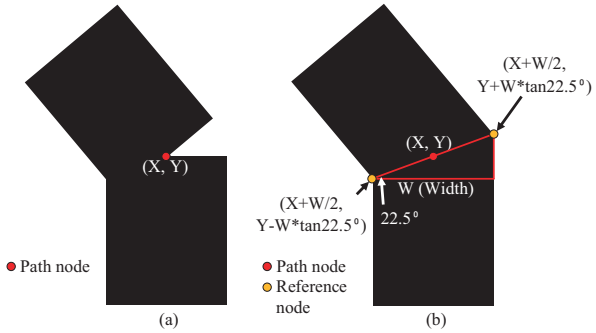

Fig. 13. (a) Schematic diagram of the 45° corner mask generation. (b) The coordinates of reference node.

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