Bottleneck Channel Routing to Reduce the Area of Analog VLSI

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Abstract - Design automation that realizes analog integrated circuits to meet performance specifications in a small area is desired. To reduce the layout area, "Bottleneck Channel Routing" is proposed in which two wires go through a routing track in the bottleneck region. A two-layer routing problem that consists of the bottleneck channel and the adjacent regions where the HV rule is not applicable is defined. The proposed algorithm uses a U-shaped routing model, and generates two-layer routing in which the number of intersections is minimized and the wire of a net includes at most one via. The obtained routing contains no conflicts if the algorithm outputs a feasible solution.

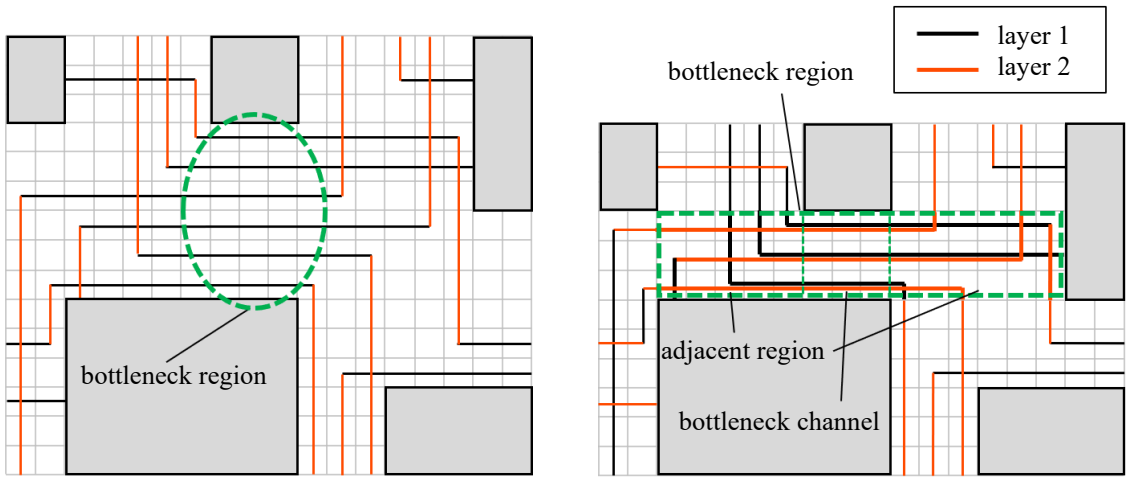
I. Introduction

Analog VLSI uses a circuit architecture with high tolerance to variation and noise and must meet various performance specifications such as current, voltage, phase, cutoff frequency, and signal waveform. The analog layout design is required not to deteriorate the circuit performance. On the other hand, it is important to realize a layout in a small area while meeting performance specifications to reduce manufacturing costs. The objective of our research is to develop a routing framework that enable us to layout a circuit in small area while meeting performance specifications.

The circuit size of analog VLSI is typically smaller than that of digital VLSI. Analog VLSI often uses fewer routing layers than digital VLSI. In VLSI with fewer routing layers, cell-based design where the routing area is defined between cells is often adopted. In various design flows for cell-based design [1], the routing area is partitioned into small routing regions called channel or switchbox, and various routing algorithms for such regions have been proposed [2,3,4].

A design flow without repeating design is preferred [5,6,7]. A routing design flow with two-layer HV routing without repeating routing design in which the routing in each layer consists of horizontal segments (H) or vertical segments (V) has been established. However, the obtained layout may contain a routing region which is a bottleneck for area reduction. The layout area may be reduced if two wires go through a routing track in such a *bottleneck region* (Fig. 1(a)) and the height of the bottleneck region is reduced.

In this paper, we propose *Bottleneck Channel Routing* (Fig. 1(b)). In Bottleneck Channel Routing, two wires go through a routing track in different layers in the *bottleneck channel*. Arbitrary routing is used in *adjacent regions* which is adjacent to the bottleneck channel, and HV routing is assumed in the other regions. In the following, *bottleneck channel problem* is defined, and an algorithm for a two-layer two-pin net bottleneck channel problem where pins of each net are placed on the upper boundary of the adjacent regions is



(a) HV Routing (b) Bottleneck Channel Routing

Fig. 1. A part of circuit layouts with the same global placement and routing

proposed.

The proposed algorithm obtains a solution in which a U-shaped routing model where the wire of each net consists of three segments is used. In a routing obtained according to the solution, the number of intersections, in case that the solution is regarded as a planer routing, is minimized, and the wire of a net uses at most one via, but conflicts may be contained. A solution is defined as feasible if no segments of different nets share the same coordinate on the same layer. Otherwise, it is defined as infeasible. Even if the algorithm outputs an infeasible solution, there exists a corresponding feasible two-layer topological routing, and a feasible routing can be obtained if vias can be inserted in the middle of segment without violations.

II. Bottleneck Channel Problem

Bottleneck channel problem (Fig. 2) is a routing problem defined on routing area that consists of a bottleneck channel and adjacent regions on both sides. The connection requirement among pins is called net. Pins of each net are placed on the boundary of adjacent regions. A wire which connects pins of a net goes through a track in the bottleneck channel, and two wires can go through a track in different layers.

If two wires intersect in the planar projection of a two-layer routing, the two wires must be assigned to different layers at the intersection. Vias must be inserted to a wire when the routing layer of the wire is changed. Note that at most one via is enough to insert between two adjacent intersections along a wire in the planar projection.

In routing design, multi-pin nets are given as an input, but a multi-pin net can be regarded as a set of two-pin nets. In the following, a basic bottleneck routing problem in which two-pin nets are given as an input is considered. In two-layer bottleneck channel problem, if each net has one pin on the boundary of each adjacent region, then the connection requirement can be satisfied by a topological routing in which at most one via is inserted for each net. To show that there is a such topological routing, in the next section, “U-shaped two-layer routing problem” is introduced.

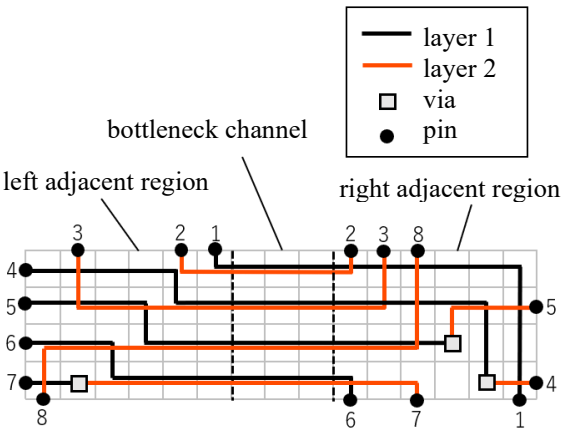


Fig. 2. Two-layer bottleneck routing

III. U-shaped two-layer Routing Problem

U-shaped two-layer routing problem which can be used to determine a feasible topological routing of a two-layer two-pin net bottleneck channel problem is discussed.

In a U-shaped two-layer routing problem, each net has one pin on the upper boundary of each adjacent region. The problem is to obtain a two-layer routing in which wires of different nets do not intersect with each other and that satisfies the following conditions.

1. The wire of each net consists of one horizontal and two vertical segments, and each segment is assigned to either layer 1 or layer 2.
2. At least one vertical segment of each net is assigned to the same layer where the horizontal segment is assigned.

In a solution satisfying the conditions above, if the two vertical segments of a net are assigned to the layer of the horizontal segment of the net, no via is inserted in the wire of the net, and if one is assigned to a different layer, one via is inserted between the vertical segment and the horizontal segment.

If a vertical segment, which is assigned to the different layer of the horizontal segment of the net, is located within the interval of the other net which is assigned to the same track, then the vertical segment and the horizontal segment of the other net share the same coordinate on the same layer, and the solution contains a conflict. Note that, however, the conflict can be resolved by inserting the via to the middle of the vertical segment, between the end of it and the next track.

In the following, U-shaped two-layer routing problem where the number of tracks is assumed to be half of the number of nets is formulated, and U-shaped routing algorithm U2TLA to solve the problem in which the track and layer assignment of segments are determined is proposed. Also, it is shown that the routing obtained according to U2TLA has no conflicts in case that U2TLA outputs a feasible solution.

In a U-shaped two-layer routing problem, the *routing area* G_m (Fig. 3) for $2m$ two-pin nets is modeled by a routing grid $(-2m \le x \le 2m, 0 \le y \le m)$ where the y-axis corresponds to the degenerated bottleneck channel, the region $x < 0$ corresponds to the *left-adjacent region*, and the region $x > 0$ corresponds to the *right-adjacent region*. A pin is placed at grid point $(x, 0)$ on the x-axis where x is an integer $(1 \le |x| \le 2m)$. A pin placed on grid point $(x, 0)$ is called *left pin* if $-2m \le x \le -1$, and *right pin* if $1 \le x \le 2m$. Each two-pin net consists of one left pin and one right pin. Track t $(1 \le t \le m)$ is the grid line connecting $(-2m, t)$ and $(2m, t)$ (Fig. 3).

Each track is assigned at most one net each on layer 1 and layer 2. The wire of a net consists of two vertical segments whose x-coordinates are the x-coordinates of pins of the net and one horizontal segment which is assigned to a track. Each segment is assigned to either layer 1 or layer 2. When segments of different nets share a coordinate, they must be assigned to different layers in a feasible solution.

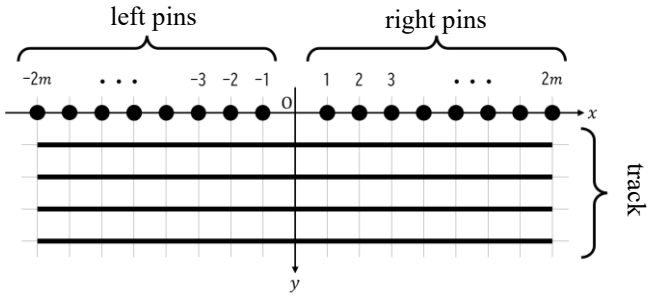


Fig. 3. Routing area $\boldsymbol{G_m}$, tracks, and pins

U-shaped two-layer routing problem

Input:

- net set $N = \{n_1, n_2, \dots, n_{2m}\}\ (m > 0)$
- $n_i = (l_i, r_i)$
  $-l_i \in \mathbb{N}^+, r_i \in \mathbb{N}^+\big(l_I < 0, r_i > 0, (\forall i \in \mathbb{N}^+)\big)$,
  $l_i \neq l_j, r_i \neq r_j\ (i \neq j, \forall i, j \in \mathbb{N}^+)$

Output:

- track assignment of horizontal segment of each net
  $A_T : N \to \{1,2,\dots,m\}$
- layer assignment of each segment
  left vertical segment $A_L : N \to \{1,2\}$
  horizontal segment $A_M : N \to \{1,2\}$
  right vertical segment $A_R : N \to \{1,2\}$

If there are various solutions that satisfies the conditions, a solution that can enable us to derive a feasible routing is preferred. Also, the following indices defined in a derived feasible routing will be used as evaluation of solutions.

1. the number of vias that are not at the end of segment.
2. the number of vias that are not at grid points.
3. the number of vias.

IV. U-shaped Routing Algorithm

In this section, we propose algorithm U2TLA for U-shaped two-layer routing problem. U2TLA selects nets one by one, determines the track assignment of horizontal segments from the upper track, and determines the layer assignment of segments. A via is inserted between a vertical segment and the horizontal segment of a net when they are assigned to different layers.

Variables and functions used in U2TLA are given below.

- t : track number
- $l(n)$: x-coordinate of the left pin of net n
- $r(n)$: x-coordinate of the right pin of net n
- $L\min(t)$: the minimum x-coordinate of the left pin of nets whose horizontal segments are assigned to layer 2 of a truck whose track number is less than t.
- $R\max(t)$: the maximum x-coordinate of right pin of nets whose horizontal segments are assigned to layer 1 of a track whose truck number is less than t.

The nets, excluding the nets whose horizontal segments are assigned to track $1 \sim t-1$, which have the following property are referred by the following variables (Fig. 4).

- $n_L(t)$: the net whose left pin x-coordinate is largest
- $n_R(t)$: the net whose right pin x-coordinate is smallest
- $n_{L2}(t)$: the net whose left pin x-coordinate is second largest
- $n_{R2}(t)$: the net whose right pin x-coordinate is second smallest

Our proposed algorithm U2TLA is given below.

U-shaped routing algorithm U2TLA

Input: net set N
Output: track assignment A_T, layer assignment A_L, A_M, A_R

Step 1. (initialization)
- $L\min(0) \coloneqq 0,\ R\max(0) \coloneqq 0$
- $t \coloneqq 1$

Step 2. (select the nets n_L, n_R to be assigned)
(A) if $n_L(t) \neq n_R(t)$
$n_L \coloneqq n_L(t)$
$n_R \coloneqq n_R(t)$
(B) otherwise $\big(n_L(t) = n_R(t)\big)$
(B1) if $l\big(n_R(t)\big) < L\min(t)$
$n_L \coloneqq n_{L2}(t), n_R \coloneqq n_R(t)$
(B2) otherwise
$n_L \coloneqq n_L(t), n_R \coloneqq n_{R2}(t)$

Step 3. (track assignment, layer assignment)
- $A_T(n_L) \coloneqq t$
  $A_T(n_R) \coloneqq t$
- $A_L(n_L) \coloneqq 1$
  $A_M(n_L) \coloneqq 1$
  $A_R(n_L) \coloneqq \begin{cases} 1 & (\text{if } R\max(t) < r(n_L) \\ 2 & (\text{otherwise}) \end{cases}$
- $A_L(n_R) \coloneqq \begin{cases} 2 & (\text{if } l(n_R) < L\min(t) \\ 1 & (\text{otherwise}) \end{cases}$
  $A_M(n_R) \coloneqq 2$
  $A_R(n_R) \coloneqq 2$

Step 4.
- $L\min(t+1) \coloneqq \min\{L\min(t),\ l(n_R)\}$
- $R\max(t+1) \coloneqq \max\{R\max(t),\ r(n_L)\}$

Step 5.
- $t \coloneqq t+1$ and stop if $t > m$
- return to Step 2.

A solution obtained by U2TLA is said to be *feasible* if no segments of different nets share the same coordinate on the same layer, and is said to be *infeasible* otherwise.

If either $n_L(t) \neq n_R(t)$, $l\big(n_R(t)\big) < L\min(t)$, or $R\max(t) < r\big(n_L(t)\big)$ is satisfied for all track t, then the solution is feasible. This will be confirmed later. In the following, track t is said to satisfy *feasible condition* if either $n_L(t) \neq n_R(t)$, $l\big(n_R(t)\big) < L\min(t)$, or $R\max(t) < r\big(n_L(t)\big)$ is satisfied. Note that if track t satisfies feasible condition, then either both n_L and n_R are set other than in Step 2(B2) or assigned $A_R(n_L) = 1$ in Step 3.

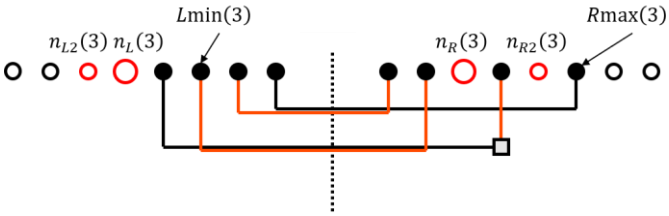
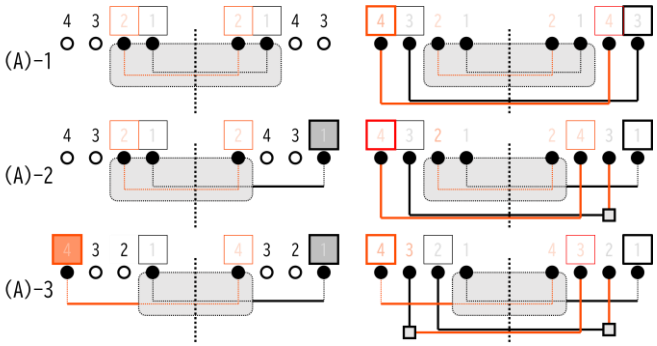
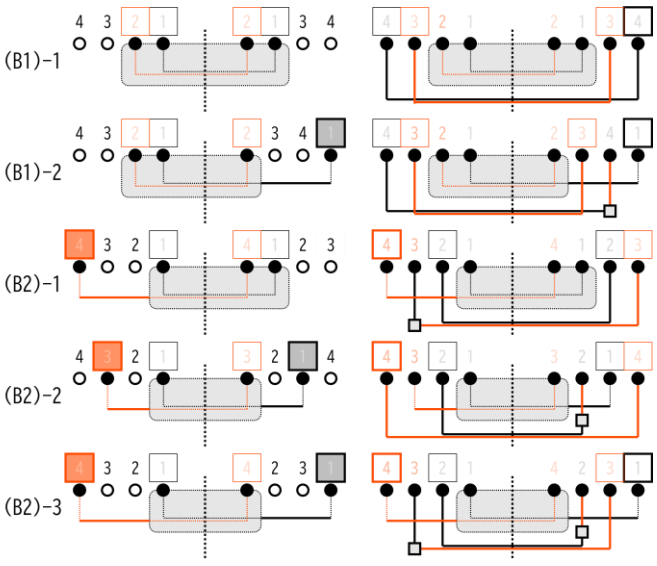


Fig. 4. Variables and functions used in U2TLA



Step 2(A)
(A)-1: 0via (A)-2: 1via (A)-3: 2via



Step 2(B)
(B1)-1: feasible (no via)
(B1)-2: feasible (right via)
(B2)-1: feasible (left via)
(B2)-2: infeasible (right via)
(B2)-3: infeasible (both via)

Fig. 5. Layer assignment in Step 3

If $l(n_R) > Lmin(t)$ in Step 3, then a via is required to insert to the wire of n_R. Similarly, if $Rmax(t) > r(n_L)$, then a via is required to insert to the wire of n_L. If via is required to insert to n_R (n_L), $Lmin$ $(Rmax)$ remains the same value in Step 4. Otherwise, it is updated by substituting the second term in Step 4.

Fig. 5 shows examples of layer assignments of segments determined in Step 3, which follows the net selection in Step 2. Fig. 5(A)-1,2,3 are the cases where a net is selected in Step 2(A). Fig. 5(B1)-1,2 and Fig. 5(B2)-1,2,3 are the cases where a net is selected in Step 2(B). The left and right figures show before track-2 assignments and the results of track-2 assignment, respectively. The black and red lines represent layer 1 and layer 2, respectively. U2TLA does not use a gray region (Fig. 5) for latter assignment. The gray region is defined as the region whose x-coordinate spans maximally so that only pins of assigned nets and the origin are contained, and y-coordinate is $1 \leq y \leq t$. A horizontal segment that extends beyond the gray region may intersect with a vertical segment of a net assigned later. In the left figures, the name of an assigned net whose horizontal segment extends to the outermost is shaded. In the right figures, the name of a net is surrounded by a thick frame if it may intersect with a vertical segment of an omitted unassigned net, and is surrounded by a thin frame if it may not.

Here, the behavior of U2TLA is shown using the example consisting of 8 nets in which the left pins belong to

$$n_1, n_2, n_3, n_4, n_5, n_6, n_7, n_8$$

and right pins belong to

$$n_2, n_3, n_8, n_5, n_4, n_1, n_7, n_6$$

in the order from the origin.

The value of each variable at t is shown in TABLE 1. Column "Step 2" in TABLE 1 corresponds to the case classification shown in Fig. 5. The symbol "*" after the value of $Lmin(t)$ $(Rmax(t))$ represents that a via is required to insert to the wire of n_R (n_L). A routing corresponding to U2TLA output is shown in Fig. 6.

TABLE 1
The behavior of U2TLA

t	n_L	n_R	$l(n_R)$	$Lmin(t)$	$r(n_L)$	$Rmax(t)$	Step 2
1	n_1	n_2	-2	0	6	0	(A)
2	n_4	n_3	-3	-2	5	$6*$	(B1)
3	n_5	n_8	-8	-3	4	$6*$	(A)
4	n_6	n_7	-7	$-8*$	8	6	(A)

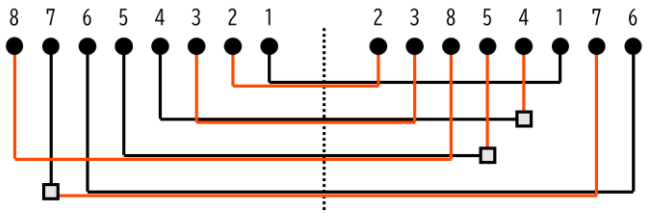


Fig. 6. A routing corresponding to U2TLA output

In the following, the validity of U2TLA is discussed. It is obvious from the definition of segments of a net that the segments of each net form a wire connecting both pins of the net. In the following, it is shown that the obtained routing has no conflicts if U2TLA outputs a feasible solution.

Let's consider a situation that the track assignment for track $1 \sim t-1$ is finished. It is shown that the following two propositions are satisfied.

(1) The wire of a net assigned to track t has no conflicts with wires of nets assigned so far.
(2) The wires of nets assigned to track t have no conflicts with each other if t satisfies feasible condition.

Note that tracks do not intersect with each other, and that a vertical grid line is exclusively used by a net.

***Lemma* 1**: The wire of a net assigned to track t has no conflicts with wires of nets assigned so far.

Proof: Each segment of net n_L selected in Step 2 has no conflicts with wires of nets assigned so far is shown.

(1-a) left vertical segment

The left vertical segment of n_L is assigned to layer 1 in Step 3, and only may has conflicts with horizontal segments in layer 1. However, the horizontal segments of all nets assigned to track $1 \sim t-1$ of layer 1 terminate to the right of the left vertical segment of n_L. If the horizontal segment of a net n assigned to the layer 1 does not terminate, then it contradicts the net selection in Step 2 since n_L should be selected before n. Therefore, the left vertical segment of n_L has no conflicts with wires of nets assigned so far.

(1-b) horizontal segment

Since wires of nets assigned so far exist in the region $y \leq t-1$, they have no conflicts with the horizontal segment of n_L on $y = t$.

(1-c) right vertical segment

The right vertical segment of n_L is assigned to layer 2 if the segment intersects with a horizontal segment assigned to layer 1, and is assigned to layer 1 otherwise. The horizontal segments of all nets assigned to track $1 \sim t-1$ of layer 2 terminate to the left of the right vertical segment of n_L because of the net selection in Step 2, and have no conflicts with the right vertical segment.

From (1-a), (1-b) and (1-c), it is confirmed that the segments of the net n_L have no conflicts with wires of nets assigned so far. Similarly, it can be confirmed that the segments of n_R selected in Step 2 have no conflicts with wires of nets assigned so far, but the description is omitted here. □

***Lemma* 2**: The wires of nets assigned to track t have no conflicts with each other if t satisfies feasible condition.

Proof: The wires of n_L and n_R assigned to track t have no conflicts with each other is shown. The segments that share coordinates among the wires of n_L and n_R are either (a) two horizontal segments or (b) one horizontal and one vertical segments.

(2-a) The horizontal segments of n_L and n_R have no conflicts with each other because they are assigned to different layers.

(2-b1) The horizontal segment of n_L (n_R) has no conflicts with the right (left) vertical segment of $n_R(n_L)$ because they are assigned to different layers from Step 3.

(2-b2) The conflict between the horizontal segment of n_L (n_R) with the left (right) vertical segment of $n_R(n_L)$ is checked in the following. In case that $n_L(t) \neq n_R(t)$, they have no conflicts because they do not share coordinates. The horizontal segment and the vertical segment share coordinates only if $n_L(t) = n_R(t)$ (see Fig. 5(B)). If either $l(n_R(t)) < L\min(t)$ (Fig. 5(B1)-1,2) or $R\max(t) < r(n_L(t))$ (Fig. 5(B2)-1), then they are assigned to different layers, and they have no conflicts with each other. Otherwise, they conflict with each other, but t does not satisfy feasible condition (Fig. 5(B2)-2,3). □

Note that a conflict occurred when feasible condition is not satisfied can be resolved by inserting the via to the middle of the vertical segment between track $t-1$ and track t.

***Theorem* 1**: A routing which satisfies the connection requirements without conflicts is obtained from the output of U2TLA in case that U2TLA outputs a feasible solution.

Proof: It is obvious from Lemmas 1 and 2 that the net assigned to track t can be realized without conflicts with wires of nets assigned so far if the solution is feasible. □

The time complexity of U2TLA is $O(m)$, since each step takes a constant time and iterated m times. In case that a net is selected in Step 2(B), other assignments may have different property on feasibility and the number of vias.

The following theorem gives a sufficient condition on inputs that have a feasible solution.

***Theorem* 2**: In the U-shaped two-layer routing problem with net set N, a feasible solution exists if there are no nets $a, b, c, u \in N$ such that

$$l(a) < l(u) < l(b), \quad r(a) < r(u) < r(b)$$
$$l(c) < l(u), \quad r(u) < r(c)$$

Proof: Let's consider a case that U2TLA outputs an infeasible solution. U2TLA outputs an infeasible solution only if t does not satisfy feasible condition for some track t. Suppose that $n_L(t) = n_R(t)$, $l(n_R(t)) > L\min(t)$, and $R\max(t) > r(n_L(t))$ are satisfied for track t. Let net u be $n_L(= n_L(t) = n_R(t))$.

The left vertical segment of u intersects the horizontal segments assigned to layer 2 of the track upper than the horizontal segment of u. There exists a net a satisfying $l(a) < l(u)$, and from Step 2, $r(a) < r(u)$.

The right vertical segment of u intersects the horizontal segments assigned to layer 1 of the track upper than the horizontal segment of u. There exists a net b satisfying $r(u) < r(b)$, and from U2TLA, $l(u) < l(b)$.

The left and right pins of a net whose horizontal segment is assigned to the same track as of u are placed outside of the left and right pins of u. There exists a net c satisfying

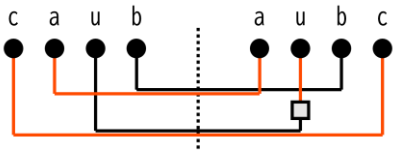


Fig. 7. An example of infeasible solution

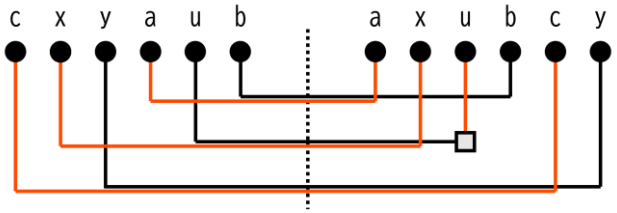


Fig. 8. A feasible routing that shows that the converse of Theorem 2 does not hold

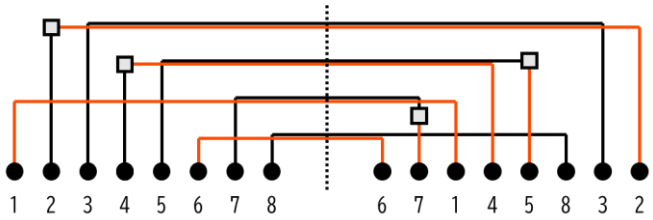


Fig. 9. A routing solution for an input that has the same pin sequence along boundary given in Fig. 6.

$l(c) < l(u), r(u) < r(c)$.

The existence of nets that contradicts to the prerequisites is shown and Theorem 2 is proved. □

Fig. 7 shows an example of an infeasible solution. In case that the number of nets is four, there are four patterns of pin sequences in which the outputs are infeasible. Even in case that the net set contains four nets violating the prerequisites of Theorem 2, a feasible physical routing may exist (Fig. 8).

A solution of the U-shaped two-layer routing problem gives a topological routing of the bottleneck channel problem. A two-layer topological routing of a bottleneck channel problem is obtained by defining a U-shaped two-layer routing problem with the same pin sequence along the boundary. In U-shaped routing problem, pins are placed on the upper boundary of the routing area. A U-shaped routing problem shown in Fig. 6 corresponds to the bottleneck routing problem shown in Fig. 2. A topological routing obtained by U2TLA could be utilized to find physical routing of the bottleneck channel problem.

Note that a topological routing obtained by U2TLA might not be fit to a physical routing of a bottleneck channel problem. A different topological routing might be obtained if other U-shaped two-layer routing problem is defined. For example, the routing problem shown in Fig. 9 is obtained in which the pins are placed on the lower boundary without changing their order from the problem shown in Fig. 2. The routing solution shown in Fig. 9 is obtained by U2TLA by assigning track from below with different net selection order. Two solutions obtained may have different track assignments and different the number of vias. It is also possible that one is feasible and the other is infeasible. This flexibility will help us to have more options when considering physical routing of a bottleneck channel problem.

V. Summary and Conclusions

In this paper, bottleneck channel routing is proposed to reduce the layout area of Analog VLSI. For the two-layer bottleneck channel problem with 2-pin net, we proposed algorithm U2TLA which obtains a routing in which the wire of a net uses at most one via. A feasible physical routing is obtained by the track assignment and the layer assignment in U2TLA if all pins are placed on the upper boundary of the routing area and U2TLA outputs a feasible solution.

Our future works are to develop an algorithm for physical routing from the topological routing obtained by U2TLA, extension to the multi-pin net problem, and extension to three or more routing layers. The routing shown in Fig. 2 is obtained from the topological routing obtained by U2TLA for the U-shaped physical routing problem shown in Fig. 6. In physical routing, we will be requested to take care the total wire length, crosstalk, and so on.

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