An Implementation of Self-Testable Layout-Level Scan C-element

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Abstract— Design methodology with asynchronous circuit is used for recent VLSI designs since it can solve several problems with synchronous circuit designs. However, manufacturing test for asynchronous circuits is more difficult than that for synchronous circuits, in which global synchronization is controlled by clock signal lines. To solve the above serious problem for dependability, a full scan design for asynchronous circuits is an answer. A transistor-level circuit for the scan C-element has also been proposed so that one way as an implementation full scan. However, there is no layout-level design of scan C-element to fabricate the chip, and no physical information is available. In this paper, we propose a layout design for scan C-elements using a Rohm 0.18µm process transistor model with a view to fabricating chips for experiments.

I. Introduction

Since asynchronous circuits can solve the clock skew problem and achieve low-power operation, VLSI design method using asynchronous circuits is attracting much attention [1,2]. Ansynchronous CAD tools such as Balsa [3] and Petrify [4] have been developed for logic synthesis of asynchronous circuits. The automatic design flow using CAD tools realize the design for practical asynchronous circuits. However, manufacturing test of asynchronous circuits is more difficult than that of synchronous circuits. There are two factors of difficulties. First, asynchronous circuits operate with a handshake protocol that uses control signals to regulate their operation (no global clock signal). Another is that a variety of sequential elements are used in various asynchronous circuits depending in their applications.

Since VLSI manufacturing test is the process of identifying defective chips before shipment, "test" is the most important step for improving chip reliability. VLSI manufacturing test determines whether a circuit is defective or not. If there exists a fault in the circuit, an erroneous value might be manifested to the outside. The error might cause failure with expected works. The expected value at the output of the circuit can be calculated by simulating the output response with applying the test pattern to the circuit without any fault. The expected value is also obtained by a good machine simulation. In addition, the test patterns generated for a manufacturing test can be evaluated. The fault coverage and fault efficiency are used as indexes to evaluate the quality of the test patterns. Fault coverage is defined as the ratio of detected faults among all the faults in the circuit. Fault efficiency is defined as the ratio of detected faults among theoretically detectable faults in the circuit. The high quality test can be achived if a set of test pattern with high fault coverage/efficiency is generated. For sequential circuits, test generation is nearly impossible due to the huge amount of computation time required. Generating test patterns achieving a high fault coverage in a realistic amount of time is reckless challenge. This problem can be solved with full scan design.

Full scan design is the de-facto standard design for testability method for synchronous circuits containing sequential elements (D-FFs). Combinational circuits are only needed to consider an input pattern at a given time. Full Scan design replaces sequential elements in a circuit with the corresponding scan elements and connects each scan element with one signal line. These paths, connected like shift registers, are called scan chains. Implementing a scan chain allows a sequential circuit can be tested as a combinational circuit without the sequential elements. On the other hand, the development for de-facto standard of test methodology is a critical challenge to popularize the design of asynchronous circuits.

To achieve high quality test for asynchronous circuits, some scan design method have been reported [5–13]. H.Hulgaard et al. [5] and S.Zeidler et al. [6] introduced a full scan design which a scan element used in Level Sensitive Scan Design (LSSD) of synchronous circuits is inserted so as to cut all feedback loops. However, inserting a large number of LSSD scan elements results in large area and delay overhead. Moreover, partial scan design methods [7,8] are proposed to reduce the number of inserted scan elements. Beest et al. [9,10] proposed an L1L2*full scan design method using scan C-elements to reduce the area and delay overhead. However, these full scan design[9,10] could not detect some specific faults. Therefore, Iwata et al. [11] proposed "Bipartite full scan

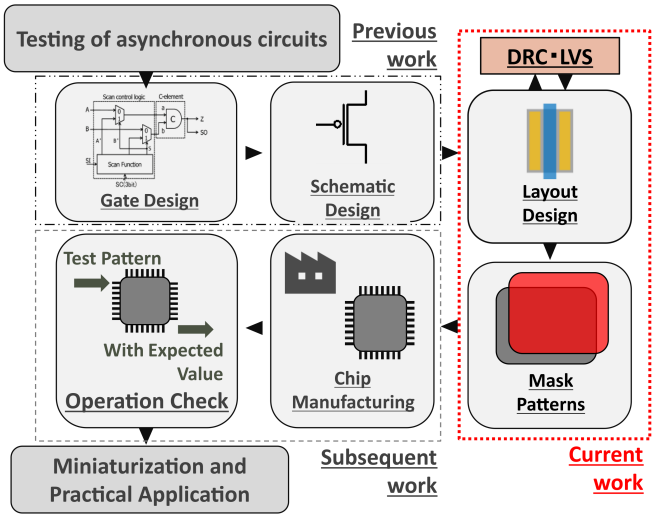

Fig. 1. Designflow of layout level scan C-element

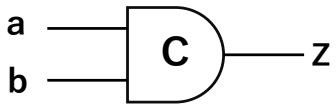

Fig. 2. C-element symbol

TABLE I
FUNCTION TABLE

a	b	Z+
0	0	0
0	1	Z
1	0	Z
1	1	1

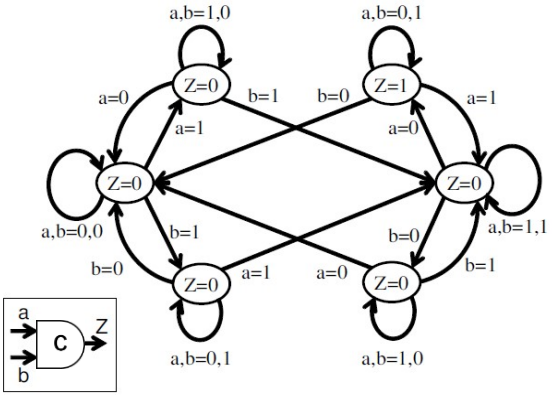

Fig. 3. State diagram of a C-element

design" which guarantees the complete test (fault efficiency = 100%) for the combinational circuit and scan C-elements in the asynchronous circuits. Since the scan C-element proposed in [11] was designed in the gate-level, enhanced transistor level scan C-element was proposed in [12]. Moreover, Shintani et al. [13] reduced the number of transistors composing the scan C-element by removing some redundant transistors. However, these scan C-elements are only up to the transistor level, none of the related studies has proposed a scan C-element with layout design. Thereby, the operation has not been verified using a real chip. In this state, the proposed scan C-element at the transistor level are not available to designers. In order for the designer to adopt the proposed scan design, a layout design of the scan C-element, which is a full-custom designed circuit, is necessary. Additionally, the designer's clear confidence cannot be obtained without operational verification using an actual chip. The ultimate goal of this research is to verify the operation of the scan C-element on a real chip to obtain reliability. In this paper, we propose a layout-level scan C-element as a preliminary step for real chip fabrication.

Fig.1 shows that, the positioning of this paper is in the process of generating mask patterns from layout design. In this paper, we propose a layout design of the transistor level scan C-element proposed in [13]. The layout design follows the design rules defined by the Rohm 0.18µm process model. Moreover, the mask pattern must be generated by clearing layout checks such as DRC (Design Rule Check) since the mask pattern is necessary when requesting chip manufacturing. As subsequent work, chips will be fabricated using the mask patterns and the operation of the chip by applying input signal voltages to the chip using an FPGA. Section II describes the functions and roles of the scan C-element. Section III describes the proposed layout design of the scan C-element. Section IV provides a summary of this paper.

II. Scan C-element

This section describes the function and roles of the scan C-element.

A. C-element

C-element is one of the most common sequential element used in asynchronous sequential circuits. The C-elements are often used for waiting states and handshake of registers. The C-element updates its internal state by obtaining signals from its input pins according to a notated state Table I. Fig.2 shows the logic symbol of the C-element. The C-element resets the value when (A,B) is (0,0), sets the value when (A,B) is (1,1), and holds the previous value otherwise. Fig.3 shows the state diagram of the C-element.

B. Function and role of the scan C-element

Fig.4 shows the the scan control logic proposed in [12]. In Fig.4, the scan C-element is composed of two parts, the scan control logic and the C-element. The scan control logic is a combinational circuit that has the function shown in Table II. In Table II, there are four types of operations. (1)Functional operation is used in the normal mode of the circuit. The inputs A and B from the input

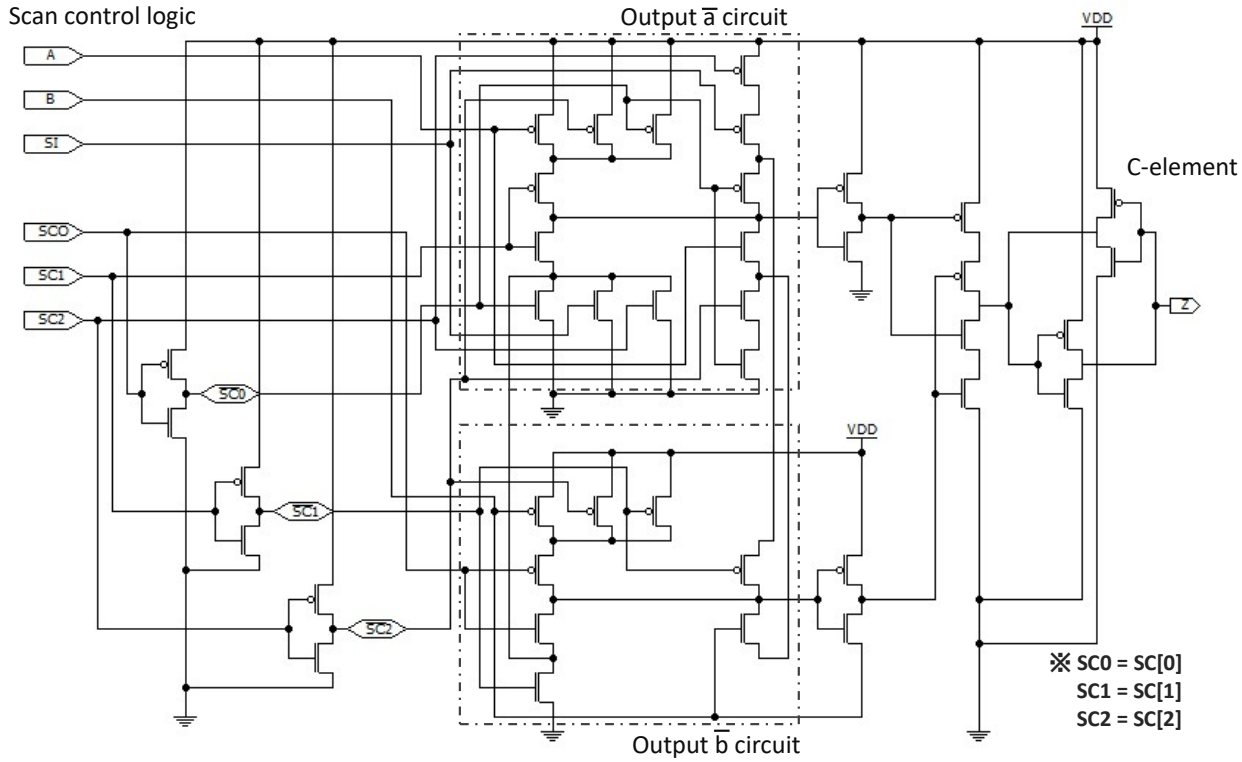

Fig. 5. Conventional scan C-element transistor-level circuit [13]

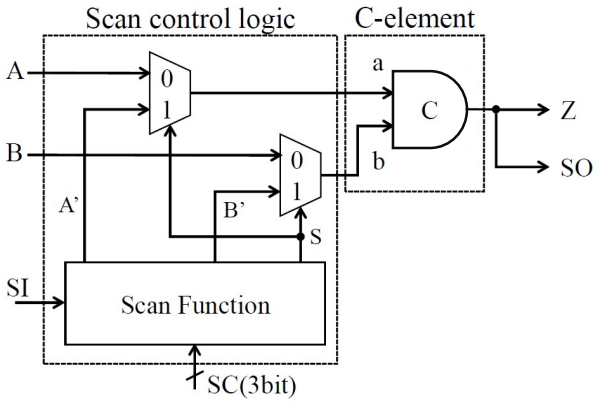

Fig 4. Scan C-element logic circuit

TABLE II
TRUTH TABLE FOR SCAN CONTROL LOGIC

SC[2:0]	a	b	usege
000	A	B	Functional operation
001	0	1	Scan operation (hold)
010	1	0	Scan operation (hold)
011	SI	SI	Scan operation (load)
100	0	0	Scan operation (set)
101	0	1	Scan operation (hold)
110	1	0	Scan operation (hold)
111	1	1	Scan operation (set)

of combination circuit are captured into the C-element, (a,b) = (A,B). (2)Hold operation is used to hold the value captured in the C-element by applying (a,b)=(0,1) or (a,b)=(1,0). (3)Load operation is used to propagate test patterns and error. By applying (a,b)=(SI,SI), the value of SI can be captured in the C-element through the scan chain. (4)Set operation is used to set the output of the C-element to 0 and 1 by applying (a,b)=(0,0) and (a,b)=(1,1) respectively. To avoid the race associated with signal switching during scan shift, there are four types of hold functions. These hold functions can be changed from non-hold functions by changing one bit of the input SC. Therefore, the race can be prevented because two or more SC signal lines are not changed at the same time.

C. *Transistor-level circuit of scan C-element*

Fig.5 shows the transistor-level circuit of the scan C-element proposed in [13]. The circuit consists of two modules: the scan control logic and the C-element. The scan

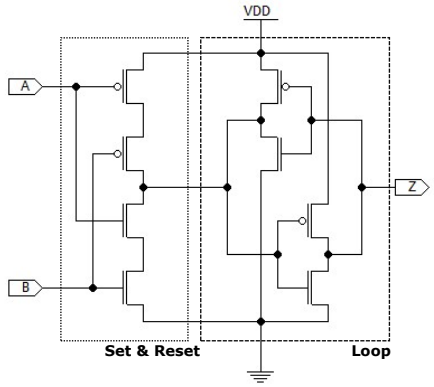

Fig. 6. Martin's CMOS transistor topology for C-element [14]

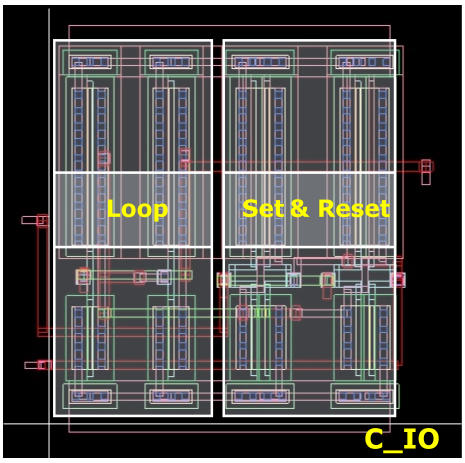

Fig. 7. Physical layout at the cell level for the evaluated C-element in the Rohm 0.18µm technology

control logic consists of two circuits, an "output $\overline{a}$ circuit" and an "output $\overline{b}$ circuit", and both circuits are designed with CMOS logic. The scan C-element consists of the transistor-level circuit proposed in [14]. The C-element input pins of C-element, has as inputs $\overline{a}$ and $\overline{b}$, which are the inverse values of a and b. Since, the proposed scan C-element was not manufactured on a chip, there is no layout-level design to fabricate the chip, and no physical information is available.

III. Proposed layout level C-element

This section, we propose a layout design of the transistor level scan C-element [13, 14] to fabricating an experimental chip. The proposed scan C-element is designed at the layout level using a Rohm 0.18µm process transistor model with manual placement and routing. We used 5µm and 2 µm as the size of channel width for pmos and

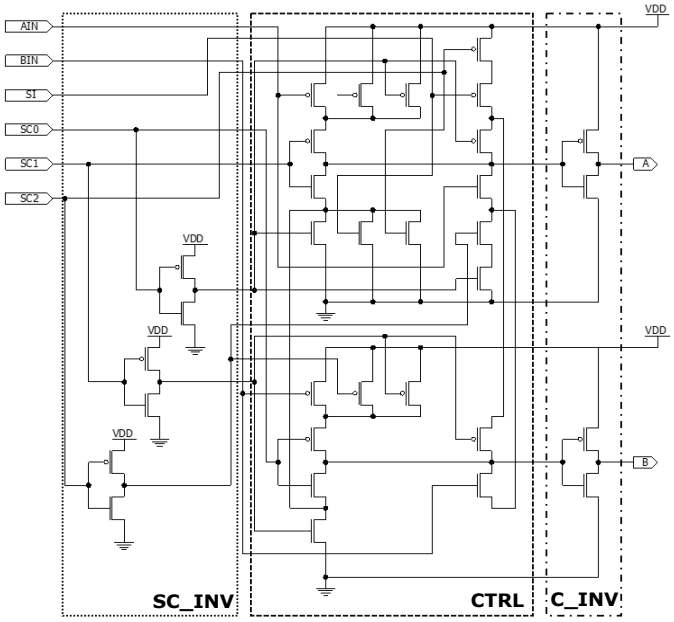

Fig. 8. CMOS transistor topology for the scan control logic [13]

nmos, respectively. The tool used for the layout design was Cadence Virtuoso Layout Editor GXL.

A. C-element

Various C-element structures have been proposed [14–16]. In this paper, we employed the simplest structure, Martin's C-element [14]. The topology of Martin's C-element is shown in Fig.6. Martin's C-element needs to the fanout capacity of the set/reset part must be larger than that of the loop part. In this design, the set-reset section is arranged in two parallel rows to satisfy the fanout capability constraint. Fig.7 shows the layout of the C-element used for the scan C-element. The floor area of "Loop" is 54.56µm^2, that of "Set&Reset" is 66.82µm^2, and the total area is 128.78µm^2.

B. Scan control logic

The transistor-level circuit of the scan control logic is designed manually to facilitate testing. In designing the layout of the scan control logic, careful manual placement and routing is necessary to ensure that the electrical characteristics are functionally equivalent to those defined in the transistor-level circuit. Fig.8 shows the transisor level circuit divided fanctionally into 3 block. The layout of the the scan control logic is designed in three major floors, SC_INV, CTRL and C_INV is shown in Fig.9. SC_INV and C_INV are simple floors consisting only NOT gates. Hence, update, delete, improvement, and other modification of the gates on these floors are flexible. The CTRL floor is designed to be independent since it is combined

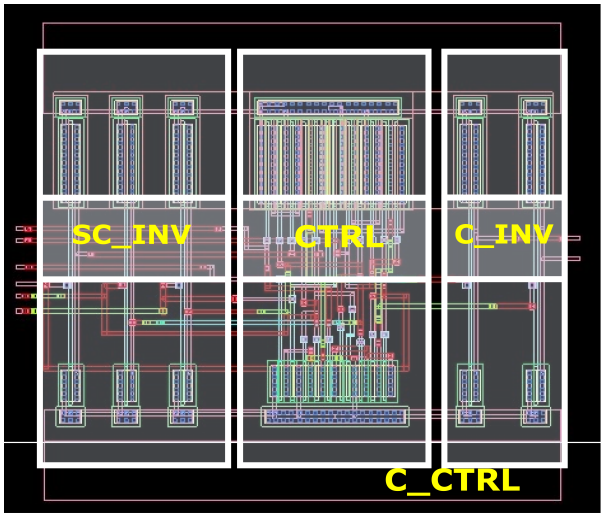

Fig. 9. Physical layout at the cell level for the evaluated the scan control logic in theRohm 0.18µm technology

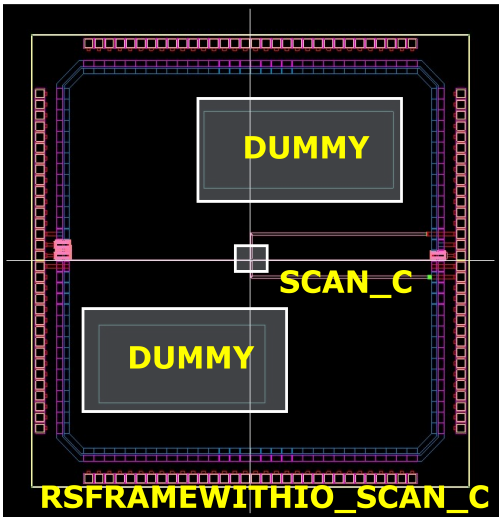

Fig. 11. Physical layout at the chip level for the C-element in the Rohm 0.18µm technology

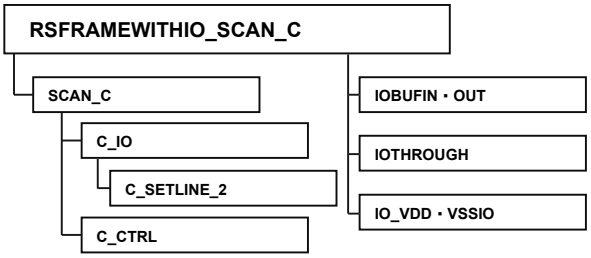

Fig. 10. Hierarchical design model for scan C-element

SC and $\overline{SC}$ signals to simplify in the transistor level. In the floor, the roles of "Functional operation" and "Scan operation" shown in Table.II are divided according to the received SC signal. SC_INV is a floor that provides both the SC and $\overline{SC}$ signals required to implement the input specification of CTRL floor. In C_INV, NOT gates are placed to match the input of the C-element in Fig.7. This function prevents inversion of the output value of the C-element. The floor area of "SC_INV" is 190.14µm^2, that of "CTRL" is 206.45µm^2, that of "C_INV" is 129.62µm^2, and the total area is 650.24µm^2.

C. *Chip layout for scan C-element*

The chip layout shown in Fig.11 was created following Rohm 0.18µm design rules of the model. The hierarchical design of the chip layout as shown in Fig.10 includes the C-element, the scan control logic and IO buffer. Dummy metal is also placed to satisfy the density rule defined in the design rule. Currently, a GDSII file showing the mask pattern is generated from the layout designed in Fig.11, and the chip manufacturing is being commissioned.

D. *Evaluation experiment*

The layout checking tools Calibre DRC and Mentor Calibre LVS (version v2021.2_18.11) are used for the verification.

- DRC (Design Rule Check): Verifies that the created layout conforms to the design rules defined by the model.
- LVS (Layout Versus Schematic): Checks wheather the layout corresponds to the electrical behavior of the schematic circuit.

The layout proposed in this paper (and the mask patterns generated from the layout) must be designed according to the design rules defined in the Rohm 0.18µm process model in order to be commissioned for chip manufacturing. Therefore, the DRC was used to verify whether there were any design rule errors in the layout. Since the final purpose our research is to verify the operation of the chip, the layout created using LVS was verified to ensure that the electrical behavior of the real chip is as functional as possible using LVS prior to manufacturing.

IV. Summary and Conclusions

Manufacturing test for asynchronous circuits is more difficult than that for synchronous circuits, in which global synchronization is controlled by clock signal lines. To solve the above serious problem for dependability, a full scan design for asynchronous circuits is an answer. A transistor-level circuit for the scan C-element has also been proposed so that one way as an implementation full scan. In this paper, we proposed a scan C-element layout as a process to guarantee the operation of the scan

C-element at the transistor level on a real chip. The chip is currently being fabricated from the mask pattern. The future work is to verify the operation of the chip by applying input signal voltages to the chip using an FPGA.

Acknowledgements

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References

[1] Wenmian Hua, Yi-Shan Lu, Keshav Pingali, Rajit Manohar, "Cyclone: A Static Timing and Power Engine for Asynchronous Circuits," In Proc. of 26th IEEE International Symposium on Asynchronous Circuits and Systems, pp.11-19, 2020.

[2] Samira Ataei, Rajit Manohar, "Shared-Staticizer for Area-Efficient Asynchronous Circuits,"In Proc. of 26th IEEE International Symposium on Asynchronous Circuits and Systems, pp.94-101, 2020.

[3] J. Spars and S. Furber, "Principles asynchronous circuit design – A Systems Perspective," Kluwer Academic Publishers, 2002.

[4] J. Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno, and A. Yakovlev, "Petrify: A tool for manipulating concurrent specifications and synthesis of asynchronous controllers," IEICE Trans. Inf. & Syst., vol.E80-D, no.3, pp.315–325, March 1997.

[5] H. Hulgaard, S.M. Burns, and G. Borriello, "Testing asynchronous circuits: A survey," Integration, the VLSI Journal, vol.19, no.3, pp.111–131, 1995.

[6] S. Zeidler and M. Krsti ´ c, "A survey about testing asynchronous circuits," In Proc. of European Conference on Circuit Theory and Design (ECCTD), pp.1–4, 2015.

[7] SA. Efthymiou, J. Bainbridge, and D. Edwards, "Test pattern generation and partial-scan methodology for an asynchronous SoC interconnect," IEEE Trans. on Very Large Scale Integr. (VLSI) Syst., vol.13, no.12, pp.1384–1393, 2005.

[8] S. Ohtake and K.K. Saluja, "A systematic scan insertion technique for asynchronous on-chip interconnects," Digest of papers of Workshop on Low Power Design Impact on Test and Reliability, pp.12–13, May 2008.

[9] Frank te Beest, Ad Peeters, Kees Van Berkel, and Hans Kerkhoff. "Synchronous full-scan for asynchronous handshake circuits," Journal of Electronic Testing, Vol. 19, No. 4, pp. 397–406, 2003.

[10] Frank te Beest and Ad Peeters. "A multiplexer based test method for self-timed circuits," In Proceedings of the 11th IEEE International Symposium on Asynchronous Circuits and Systems, pp. 166–175, 2005.

[11] Hiroshi Iwata, Satoshi Ohtake, Michiko Inoue and Hideo Fujiwara, "Bipartite Full Scan Design: A DFT Method for Asynchronous Circuits," In Proc. of IEEE 19th Asian Test Symposium (ATS'10), pp.206-211, Dec. 2010.

[12] Mamoru Ishizaka, Ken'ichi Yamaguchi, Hiroshi Iwata:"Race-free and O(n) asynchronous scan path test method," IEICE Transactions, Vol.J102-A, No.6, pp.172-181 , Jun. (2019) in Japanese.

[13] Yuta Shintani, Ken'ichi Yamaguchi, and Hiroshi Iwata, " An Implementation of Functional Speed Oriented Transistor-Level Scan C-element, " In Proc. of Workshop on RTL and High Level Testing 2021, TS3-2, pp.1-5, Nov. (2020)

[14] A.J. Martin, "Formal program transformations for VLSI circuit synthesis," in Formal development programs and proofs, pp.59–80, Addison-Wesley Longman Publishing, 1989.

[15] I.E.Sutherland, "Micropipelines." Communications of the ACM, 32, Jun. 1989, pp. 720-738.

[16] K.van Berkel, "Beware the isochronic fork." Integration, the VLSI Journal, 13(2), Jun. 1992, pp. 103-128.

[17] K.Konishi, S.Kishimoto, B.-Y.Lee, H.Tanaka, K.Taki,"A logic synthesis system for the pass-transistor logic SPL," In Proc. of The 24th Workshop on Synthesis And System Integration of Mixed Information technologies ' 96, pp.32–39 (1996).