Evaluation of FPGA performance in a cryogenic environment

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Abstract - Quantum computers are a new type of computer that use quantum mechanics to perform massively parallel computations. The superconducting quantum computer is the most promising method for practical use because it is easy to control and has high integration. To use quantum computers, a classical computer is needed as the controller. We are studying how FPGAs perform in cryogenic environments to determine if we can use them to control a superconducting quantum computer. Initially, we test FPGAs made by Xilinx and Altera to see how they operate at temperatures as low as -150°C. Then, we evaluate the performance of FPGAs in cryogenic environments by measuring the oscillation frequency of ring oscillators, power consumption, phase-locked loops (PLLs), and macro-CPUs.

I. Introduction

Quantum computers are a new type of computer that uses the principles of quantum mechanics, such as quantum superposition and quantum entanglement, to perform massively parallel computations. It is known that quantum computers can efficiently solve some problems that cannot be solved by classical computers. Quantum computers also hold great promise in the fields of quantum simulation and machine learning.

Any two-state quantum mechanical systems can be used to build a quantum computer. Among these, the superconducting quantum circuit is a method to realize a quantum bit by placing a quantum circuit in a cryogenic environment (about 10mK), and is expected to be the most promising method for practical use because it is easy to control and has high integration [1].

Quantum computers using these superconducting quantum circuits, or superconducting quantum computers, have made rapid progress in the past few years in terms of both their hardware and software. In Japan, a second superconducting quantum computer developed domestically in 2023 [2], and research is being actively conducted in many countries.

In using these quantum computers, quantum-classical hybrid computing is being considered, in which multiple quantum computers and classical computers are used in a cluster, and classical computers are used as control electronics.

In the superconducting quantum systems implemented today, a classical computer is installed in a room temperature environment and connected by cables to each quantum bit in a superconducting quantum circuit in a refrigerator. However, due to the increasing number of cables and the influx of heat from the cables, there is a need for the classical computer to also operate in a cryogenic environment. Since the latency is also limited by cables, it is desirable to operate in a cryogenic environment up to the control to achieve higher computational speeds [3].

In this study, we evaluate the performance of FPGAs, which are expected to be used as control electronics for quantum computers thanks to their reconfigurability and high parallel processing capability, in a cryogenic environment. We confirm the operation of the FPGA itself and basic circuits such as UARTs, FIR filters, and PLLs that are needed to control quantum computers, and then evaluate ring oscillators and macro-CPUs to assess the performance of FPGAs in cryogenic environments.

Section II explains MOSFET characteristics in cryogenic environment. Section III and section IV explain the measurement method of the supposed FPGAs and their results, respectively. Section V provides a discussion of the measurement results, and finally Section VI provides overall conclusion.

II. MOSFET in cryogenic environments

MOSFET characteristics are highly dependent on temperature. This is also true in cryogenic environments. Therefore, this section aims to summarize the characteristics of MOSFETs and digital circuits in cryogenic environments, especially in 4K environments, to clarify the characteristics of FPGAs in cryogenic environments.

The main characteristic changes of MOSFETs are shown below [4].

- Increasing mobility
- Increasing threshold voltage
- Decreasing sub-threshold slope

First, let us discuss the increase in mobility. The mobility in silicon is mainly limited by scattering effects in the lattice. it is dominated by phonon scattering at high temperatures, and by Coulomb or ionized impurity scattering at lower temperatures. Since phonon scattering is generally dominant

at higher temperatures, the mobility increases in low-temperature environments [4].

Next, let us discuss the increase in threshold voltage. As the temperature decreases, the potential to turn on the MOSFET increases because the thermal energy available to the carriers is reduced. This corresponds to an increase in the threshold voltage. Using the 28nm process nMOS in the previous study as an example, it was confirmed that the threshold voltage increases by approximately 16mW as the temperature decreases from 300K to 4.2K[5].

Finally, let us discuss the Decrease in sub-threshold slop. The sub-threshold slope is a measure of the drain voltage step required to increase the drain current by one decade for a device working below its threshold voltage. The ideal sub-threshold slope can be approximated by the following equation

$$SS = \ln(10)\frac{kT}{q}$$

where k is Boltzmann constant, T is the absolute temperature and q is the electron charge. At 300K, the sub-threshold voltage is indeed close to its ideal value of 60 mV/dec and is proportional to temperature. Therefore, the above equation indicates that the sub-threshold slope is greatly reduced in cryogenic environments.

III. Measurement methods

In this research, the following evaluation boards are used.

- ARTY A7(Xilinx Artix-7)
- ZYBO Z7(Xilinx Zynq)
- PYNQ Z1(Xilinx Zynq)
- DE0-CV (Altera Cyclone-V)
- DE0(Altera Cyclone-III)

The specifications of these evaluation boards are shown in TABLE I.

TABLE I
The specification of evaluation boards

(a)Xilinx FPGA

Evaluation board	ARTY A7	ZYBO Z7	PYNQ Z1
FPGA	Artix-7	Zynq-7000	Zynq-7000
Technology [nm]	28	28	28
Process	TSMC 28HLP	TSMC 28HLP	TSMC 28HLP
Temperature range [°C]	0 - 85	0 - 85	0 - 85

(b)Altera FPGA

Evaluation board	DE0	DE0-CV
FPGA	Cyclone-III	Cyclone-V
Technology [nm]	65	28
Process	TSMC 65LP	TSMC 28LP
Temperature range [°C]	0 - 85	0 - 85

The evaluation boards are placed in a freezer (NIHON FREEZER CO., LTD. CLN-1700CWE) to assess the performance of the FPGAs within a temperature range of 0°C to -150°C. The FPGAs are connected to a PC in a room-temperature environment via a USB cable and programmed using a JTAG interface. The USB 3.1 tester (AVHzY CT-3) is utilized to measure the power consumption of the FPGA and determine the overall evaluation board's value. Jumper wires are employed to observe the output signals of the FPGA using an oscilloscope (Tektronix MSO3034).

A. Operation confirmation

Following circuits are evaluated in the above FPGAs.

- UART
- FIR filter
- Ring oscillator (301 stages)
- PLL, MMCM
- MicroBlaze
- Cortex A9 Processor in Zynq
- Nios II

The UART circuit transmits and receives 8-bit data. The FIR filter takes 16-bit data as input, performs filtering on it, and issues the corresponding 32-bit data as output. The PLL and MMCM maintain the input clock signal at its original frequency and generate signals multiplied by 2 and divided by 1/2, without performing any phase adjustment. In a macro-CPU such as MicroBlaze, a “while loop” is configured in the program, and it operates GPIO and UART within the loop.

B. Performance evaluation

The power consumption for the above circuits is measured. Measurements are taken every 10℃ decrease between 0℃ and -150℃.

To evaluate the ring oscillator, the inverter delay is measured in addition to the power consumption. This inverter delay t can be obtained from the value of the oscillation frequency f[Hz], which can be observed with an oscilloscope, using the following equation.

$$t = \frac{1}{2 \cdot 301 \cdot f}\ [\mathrm{s}]$$

In ARTY A7 we also create and evaluate ring oscillators placed and routed manually and compare their characteristics with those of ring oscillator placed and routed automatically. Fig. 1 and Fig. 2 show the layout results of the ring oscillators. For the manually placed and routed ring oscillator, we create a circuit with a short wiring length by placing LUTs (Look Up Tables) side by side. In Fig. 2, the white lines represent connected wires between the adjacent LUTs. As a result, the wiring length is adjusted as almost the same short length.

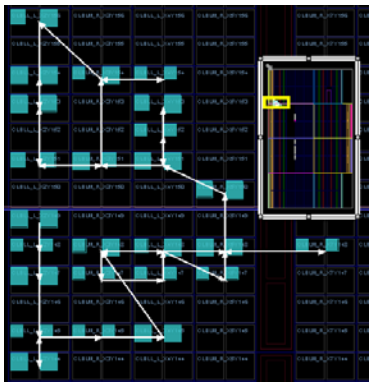

Fig. 1. Layout of ring oscillator placed and routed automatically.

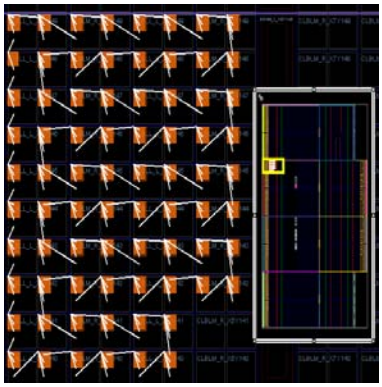

Fig. 2. Layout of ring oscillator with a short wiring length.

For the macro-CPUs such as MicroBlaze, we evaluate the availability in a cryogenic environment by checking the operating speed and timing errors during the execution of the Dhrystone benchmark. The default clock frequencies for MicroBlaze, Cortex-A9, and NiosII are 100MHz, 667MHz, and 50MHz, respectively. Here, we also evaluate the power consumption of the soft macro-CPUs operated with a lower clock frequency than the default frequency in the -150℃ environment.

IV. Measurement Results

A. Operation confirmation

It is confirmed that ARTY A7, DE0-CV, and DE0 properly operate in -150℃. In addition, these evaluation boards can be restarted by reconnecting the cable. Regarding ZYBO Z7, it is basically possible to write and operate circuits even in -150℃, but initialization for the Cortex A9 processor becomes impossible at -110℃. All functions of PYNQ Z1 stopped at -110 ℃, so it is impossible to evaluate it in the lower temperature environments.

For the synchronous circuits validated in this study, it is observed that even in a cryogenic environment, they performed similarly to how they do in a room temperature environment when the FPGA itself remained operational. Here, since the PLL and MMCM signals are transmitted through long jumper wires, resulting in distortion of high-frequency signals, it is impossible to evaluate the waveforms visually on an oscilloscope. Therefore, the operation is evaluated by inputting the signal generated by the PLL and MMCM as a clock signal to the UART circuit, which has been previously confirmed to operate even in a cryogenic environment, and checking whether the UART signal is correctly issued. The results of these operations are summarized in TABLE II.

TABLE II
The result of operations for each FPGA

		Xilinx			Altera	
		ARTY A7	ZYBO Z7	PYNQ Z1	DE0-CV	DE0
Operation		○	○	×	○	○
Write circuits		○	○	×	○	○
UART		○	○	×	○	○
FIR filter		○	○	×	○	○
Ring oscillator		○	○	×	○	○
PLL		○	○	×	○	○
MMUM		○	○	×	○	○
MicroBlaze	Initialization	○	–	–	–	–
	Run	○	–	–	–	–
Cortex A9 processor	Initialization	–	×	×	–	–
	Run	–	○	×	–	–
Nios II		–	–	–	○	○

B. Performance evaluation

Power consumption is measured while the circuit evaluated is operating. Since all the circuits show the same characteristics when the same evaluation board is used, only the change in power consumption of the ring oscillator is shown in from Fig. 3 to Fig. 7 as a representative example. In these figures, the horizontal axis is the internal temperature of the freezer, and the vertical axis is the power consumption, with the leftmost result being the measurement result in a low temperature environment. In the temperature range measured in this study, the power consumption changes very little, with a maximum change of about 50 mW.

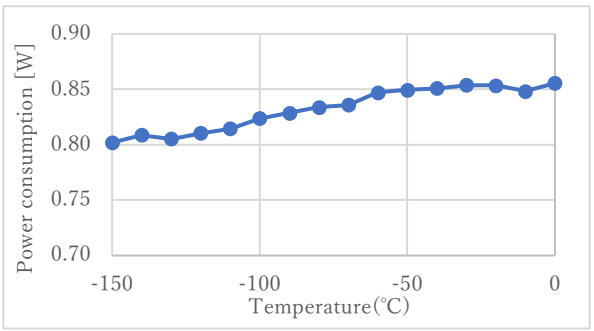

Fig. 3. Change in power consumption of ARTY A7.

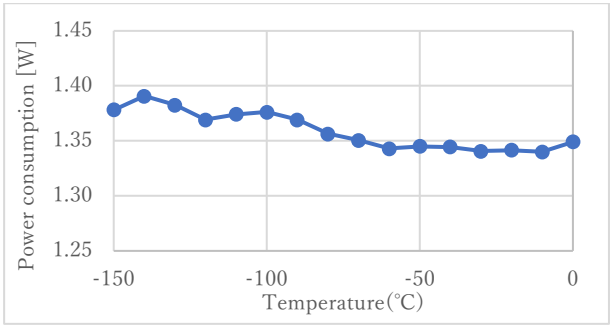

Fig. 4. Change in power consumption of ZYBO Z7.

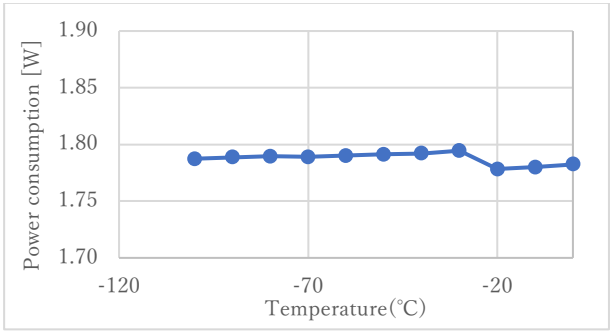

Fig. 5. Change in power consumption of PYNQ Z1.

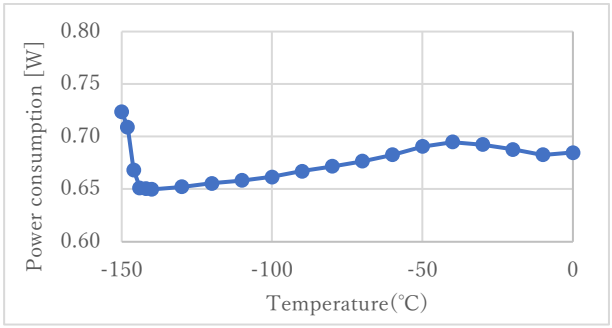

Fig. 6. Change in power consumption of DE0-CV.

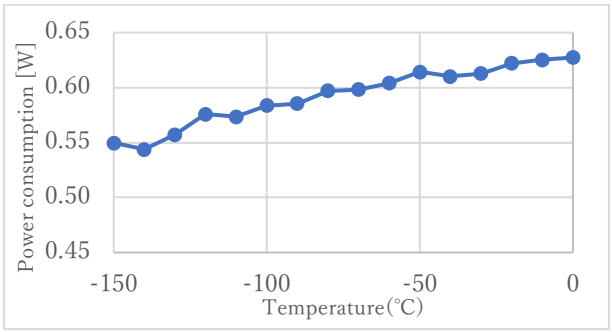

Fig. 7. Change in power consumption of DE0.

The change of inverter delay calculated from the oscillation frequency of the ring oscillator is shown in Fig. 8 and Fig. 9.

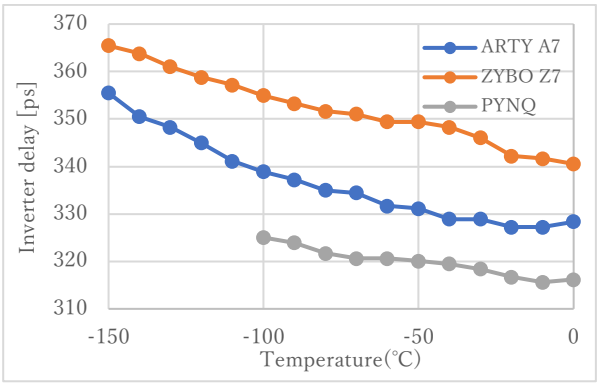

Fig. 8. Change in inverter delay for Xilinx FPGAs.

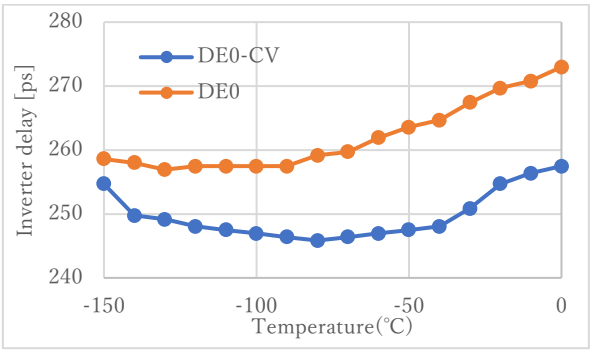

Fig. 9. Change in inverter delay for Altera FPGAs.

In Fig. 8 and Fig. 9, the horizontal axis is the internal temperature of the freezer, and the vertical axis is the inverter delay, with the leftmost result being the measurement result in a low temperature environment. During cooling, the delay for the Xilinx FPGA evaluation boards increases, while the delay for the Altera FPGA evaluation boards tends to decrease.

Fig. 10 and Fig. 11 depict the variations in power consumption and inverter delay of the ring oscillator operated in a cryogenic environment with manual placed and routed on the ARTY A7. Additionally, Table III represents the rate of change in inverter delay and power consumption for both automatic and manual circuit configurations.

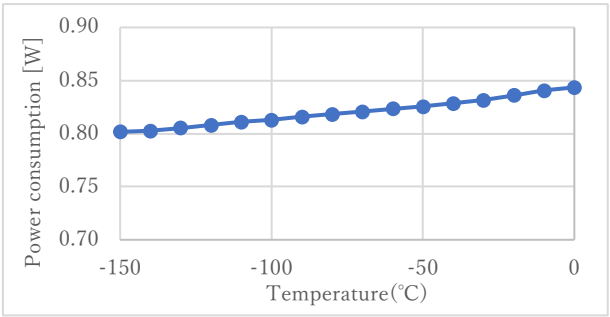

Fig. 10. Change in Power consumption of ring oscillator with short wiring length.

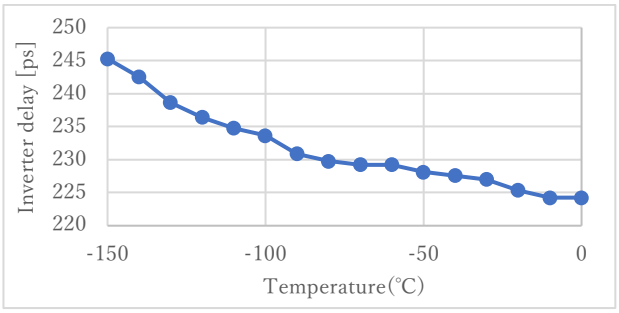

Fig. 11. Change in inverter delay of ring oscillator with short wiring length.

TABLE III
The rate of change in inverter delay and power consumption for both automatic and manual circuit configurations

	Rate of change relative to 0°C [%]	
	Inverter delay	Power consumption
automatic	+8.04	-5.94
manual	+9.38	-4.96

The results of the performance evaluation of each macro-CPU running the Dhrystone benchmark are explained as follows. The number of Dhrystone benchmark that can be executed per unit of time for all macro-CPUs was same between room temperature environment and the cryogenic environment. Therefore, no change in the performance of the macro-CPUs is observed in the cryogenic environment. Fig. 12 and Fig. 13 show the measured power consumption of Dhrystone benchmark at each clock frequency in the -150℃ environment.

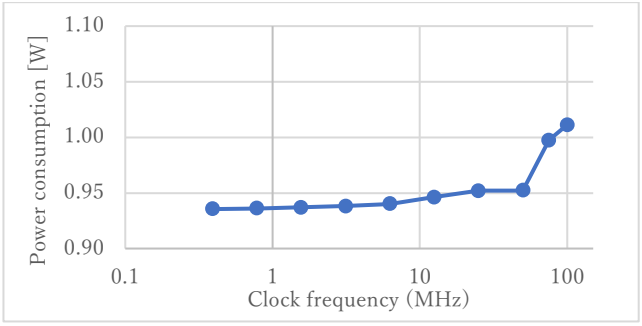

Fig. 12. Power consumption at each clock frequency for MicroBlaze.

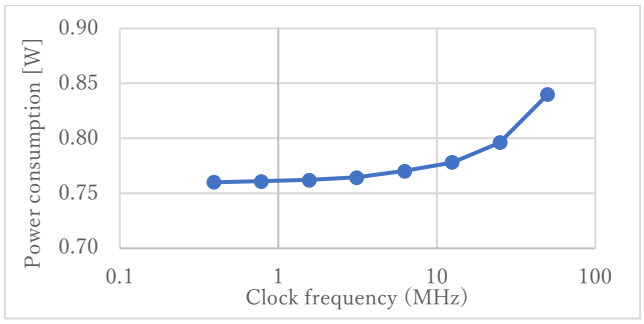

Fig. 13. Power consumption at each clock frequency for Nios II.

V. Discussion

This section commences with a discussion on the variation of the inverter delay in ring oscillators. As mentioned earlier, in cryogenic environments, the mobility of MOSFETs increases. However, the threshold voltage also rises simultaneously. This results in an increased inverter delay at lower temperatures for devices operating at lower voltages. This phenomenon is also observed in this study, where the inverter delay in Xilinx FPGAs with a low supply voltage. On the other hand, the Altera FPGA is not affected by the increased threshold voltage because it operates at a relatively high supply voltage. This result aligns with the characteristics of a ring oscillator configured as an ASIC [6], and it is anticipated that the inverter delay characteristics will similarly change around the 1V supply voltage range in FPGAs. Therefore, in the case of the Xilinx FPGAs used in this study, the increased delay in cryogenic environments is a concern. However, the results of running Dhrystone benchmark on the macro-CPUs showed that this delay variation does not affect performance in environments down to -150°C for these macro-CPUs running at standard frequencies.

Comparing the characteristics of circuits placed and routed automatically and manually in the ring oscillator, the rate of change of the inverter delay shows higher values for the manual circuits. We believe this is the result of the wiring delay becoming a smaller proportion of the total delay and the MOSFET delay becoming more dominant. The rate of change of power consumption is lower for the manual circuit. This is because the wiring is shorter and the change in power consumption due to the wiring is smaller.

Power consumption is discussed next. Since the leakage current decreases as the threshold voltage increases, the power consumption should decrease in cryogenic environments. However, the change in power consumption is small in the temperature range of this study, and the characteristics of the change differ from board to board, including the dynamic power consumption of macro-CPUs. Comparing the power consumption results of ZYBO Z7 and PYNQ Z1, which are equipped with the same FPGA, shows completely different characteristics, suggesting that the peripheral circuits have a significant impact. Thus, in this study, the cause of the FPGA

performance change cannot be identified. It can be concluded that it is necessary to find a way to measure the power consumption of the peripheral circuits, and thus the FPGA itself, to evaluate these factors.

Finally, since it is required to operate at lower power consumption in cryogenic environments, the power consumption of some macro-CPUs running at lower clock frequencies are measured. However, the power consumption does not change significantly with clock frequency. This result would be a good guideline for considering the allowable power consumption and operating constraints when the control circuit is placed near the superconducting quantum circuit in a cryogenic environment.

VI. Conclusion

This study has verified and evaluated the operation and performance of FPGAs in cryogenic environments. As the result, three FPGAs, ARTY A7, DE0-CV, and DE0, have been confirmed to operate at -150°C as well as in room temperature environments. In terms of performance evaluation, the characteristics of FPGA delay in cryogenic environments have been clarified based on the propagation delay of ring oscillators, the impact of cryogenic operation on the performance of macro-CPUs has also been evaluated.

However, since the control electronics of quantum systems require functions such as AD conversion and DA conversion, it is necessary to conduct research including the evaluation of peripheral circuits, such as whether to use FPGAs equipped with these functions or to prepare separate circuits. And since the actual control electronics of the quantum system must be installed in a 4K environment, it is necessary to evaluate the performance of FPGAs in a more practical environment using equipment that can realize a lower temperature environment.

In addition, although this study only evaluated the performance of the actual FPGA, a simulation environment would also be necessary to produce cryogenic control electronics. Therefore, one of the issues to be addressed in future research is to construct a simulation environment by clarifying the characteristics of the input/output signals between the quantum computer and the control electronics, and by modeling the operation of the electronics in the cryogenic environment.

Acknowledgements

This paper is based on results obtained from a project, JPNP16007, subsidized by the New Energy and Industrial Technology Development Organization (NEDO).

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