Reduction of Static Power Consumption of LSI by Decreasing Leakage Current Paths with Equivalent Logic Expression Conversion

Kazuma Dobata Kazuhito Ito

Graduate School of Science and Engineering
Saitama University
Saitama 338-8570, Japan

Abstract— Reducing the static power consumption of large-scale integrated circuits (LSI) has become an important issue. The main cause of static power consumption in CMOS circuits is leakage current flowing through off-state MOS transistors. In this paper, we propose a method to reduce static power consumption of CMOS LSIs by equivalently converting a given logic expression to decrease the number of leakage current paths and thereby stacking MOS transistors to reduce the leakage current.

I. Introduction

Power consumption in large-scale integrated circuits (LSIs) consists of dynamic power consumption, which is consumed when the voltage in the circuit changes according to circuit operation, and static power consumption, which is consumed by leakage current flowing through MOS transistors in a cut-off state. In recent years, with the miniaturization of integrated circuits, the power supply voltage has been lowered and the capacitance in circuits has been reduced, leading to a reduction in dynamic power consumption, but static power consumption is relatively increasing [1, 2].

In order to reduce leakage current in CMOS circuits, a method of inserting current control transistors into the circuit [5] and a method of adding feedback transistors [4] have been proposed. However, this is limited to cases where circuit operation is extremely slow. Methods have been proposed to reduce leakage current by increasing the gate length of the transistor [6] or by stacking transistors to equivalently increase the gate length [7], but these methods have the side effect of increasing the area and gate capacitance of the transistor.

Logic circuits that perform complex logical operations are sometimes implemented by combining many simple CMOS logic gates such as NAND and NOR. Circuit synthesis based on logic gate libraries tends to result in circuits like this. Each CMOS logic gate provides a path for leakage current. A circuit using a large number of CMOS logic gates has many leakage current paths, and a large amount of leakage current flows.

For a logic expression that accepts multiple input signals, we can consider a complex CMOS logic gate consisting of many transistors. A given logic equation can be implemented using a small number of complex CMOS logic gates. As the number of logic gates decreases, leakage current paths decrease, and thus the reduction of leakage current is expected. In addition, many transistors are generally connected in series in complex CMOS logic gates, and by simultaneously shutting off those transistors, it is expected that the leakage current is further reduced with stacking effect.

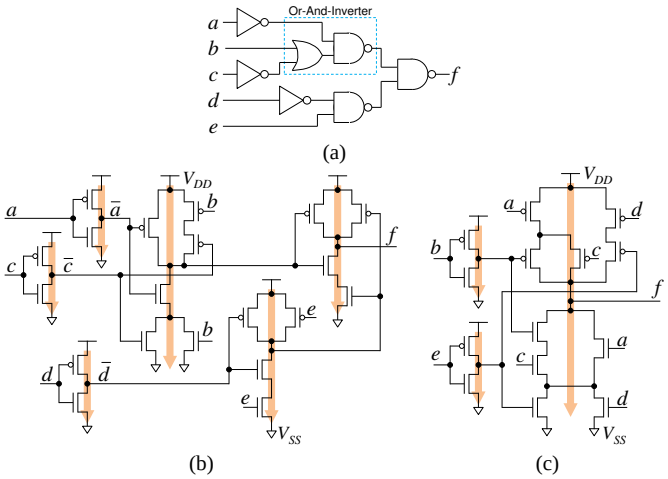


Fig. 1. Leakage current path reduction by circuit conversion. (a) an example logic circuit. (b) an implementation with primitive gates. (c) a converted circuit.

The remainder of the paper is organized as follows. A motivating example is presented in Sect. 2. The proposed method is described in Sect. 3. Experimental results are shown in Sect. 4 and Sect. 5 concludes the work.

II. Motivating Example

Consider a circuit that implements the logic function f given by Eq. (1). Assuming implementation in a CMOS circuit, the equation is transformed as Eq. (2).

$$f = \bar{a}(b+\bar{c}) + \bar{d}e \quad (1)$$

$$= \overline{\overline{\bar{a}(b+\bar{c})} \cdot \overline{\bar{d}e}} \quad (2)$$

Eq. (2) assumes the use of a composite CMOS gate (Or-And-Inverter), and corresponds to the logic circuit shown in Fig. 1(a). Fig. 1(b) shows the result of implementing the logic circuit in Fig. 1(a) using a CMOS transistor circuit. In Fig. 1(b), a path of leakage current flowing through the MOS transistors between V_{DD} and V_{SS} is shown by an orange arrow. There are six leakage current paths in the circuit of Fig. 1(b).

The logic function f of Eq. (1) can be equivalently transformed to Eq. (3).

$$f = \overline{(a+\bar{b}c)(d+\bar{e})} \quad (3)$$

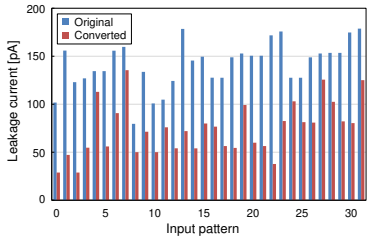


Fig. 2. The leakage current of the example circuits.

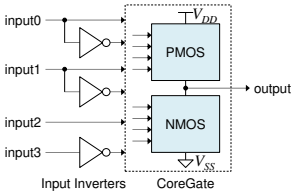


Fig. 3. The circuit structure with CoreGate.

The CMOS transistor circuit corresponding to Eq. (3) is shown in Fig. 1(c). It can be seen that the number of leakage current paths is reduced to three.

Fig. 2 shows the leakage current simulation results for the original circuit shown in Fig. 1(b) and the converted circuit shown in Fig. 1(c). Direct current (DC) analysis of the transistor circuit was performed using a circuit simulator to determine the leakage current. The simulation conditions used are the same as those used in the experiments described in Sect. 3.A. There are five inputs a, b, c, d, e, and there are $2^5 = 32$ combinations of logic values of the inputs. The combination of input values is expressed as $(a,b,c,d,e) = (0,0,0,0,0),\ldots,(1,1,1,1,1)$, and it is considered as a 5-bit binary number. Then the value (0 to 31) represents each input value combination pattern. Fig. 2 shows the leakage current values for all input patterns. It can be seen that the leakage current of the converted circuit (Fig. 1(c)) is smaller than that of the original circuit (Fig. 1(b)) for all the input patterns.

Consequently, the leakage current can be reduced by equivalently converting the logic function representing the logic circuit so as to reduce the number of leakage current paths. In addition, in the circuit that outputs f in Fig. 1(c), the number of MOS transistors connected in series between V_{DD} and V_{SS} is increased from Fig. 1(b). When the transistors connected in series are in the cut-off state, the equivalent resistance of the leakage current path increases, and it is also expected that the leakage current value itself will be reduced.

III. The Proposed Method

The proposed method consists of four techniques. The given circuit is converted into a CoreGate circuit structure to reduce leakage current paths (III.A). The leakage current of input inverters is reduced by stacking transistors (III.B). The delay of the converted circuit is reduced by optimizing the MOS transistor connections (III.C) and by widening channel width of selected transistors (III.D).

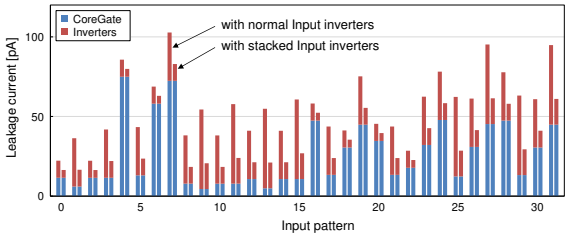


Fig. 4. Breakdown of leakage current of the converted circuit in Fig. 1(c).

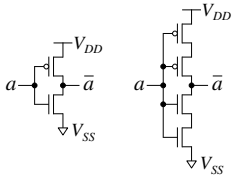


Fig. 5. CMOS inverter. (a) normal inverter (1L), (b) stacked inverter (2L).

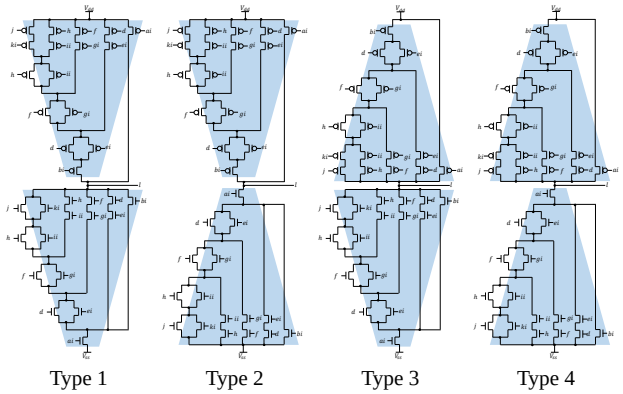


Fig. 6. Combinations of the PMOS and NMOS structures for the output l of cm85a.

A. Conversion to CoreGate structure

As a circuit structure with a small number of leakage current paths, we propose a circuit consisting of a single-stage CMOS gate (*CoreGate*) that calculates the output value and CMOS inverters (input inverter) required to invert the input signals. Fig. 3 shows the proposed circuit structure. The circuit shown in Fig. 1(c) consists of one CoreGate on the right side that calculates the output f, and two input inverters that calculate the inverse of the inputs b and e. As shown in Eq. (3), the logic function representing CoreGate performs the entire inversion on a logic expression that combines an arbitrary number of stages of AND and OR for input variables or their inversions. A given logic function is equivalently converted into a logic function in this form, and a circuit with the proposed structure is derived. If there are multiple output values, one CoreGate is provided for each output value.

B. Reduction of leakage current of input inverters

Fig. 4 shows the breakdown of the leakage current of the circuit shown in Fig. 1(c). It can be seen that while the leakage current of the entire circuit is reduced by using CoreGate, the leakage current of the input inverters occupies a large propor-

tion. Therefore, reducing the leakage current of the input inverters has a large effect on reducing the leakage current of the entire circuit. The transistors in the input inverter are stacked to reduce the leakage current. Fig. 5 shows a normal inverter that is not stacked (a) and an inverter that has PMOS transistors and NMOS transistors stacked in two stages (b).

The result of leakage current simulation when using stacked input inverters is shown in Fig. 4. It can be seen that stacking greatly reduces the leakage current of input inverters and is effective in reducing overall leakage current. On the other hand, there is almost no effect on the leakage current of CoreGate.

C. Construction of PMOS and NMOS parts

For a given logic function, the CoreGate implementation is generally not unique. Four examples of CoreGate implementations that calculate the output l of circuit cm85a are shown in Fig. 6. The PMOS part in Type 1 is constructed so that the number of parallel connections of PMOS transistors is as much as possible on the V_{DD} side and as few as possible on the output l side. On the other hand, the PMOS part in Type 3 is constructed so that the parallel connection of PMOS transistors is as small as possible on the V_{DD} side and as large as possible on the output l side. Also, the degree of parallelism of transistors is high on the output l side and low on the V_{SS} side for the NMOS part in Type 1, but the situation is reversed in Type 2. The combination of two types of PMOS parts and two types of NMOS parts results in the four types of CoreGate implementations shown in Fig. 6. Among these various possible implementations, an implementation with desirable leakage current and delay time can be selected.

D. Transistor sizing to reduce delay

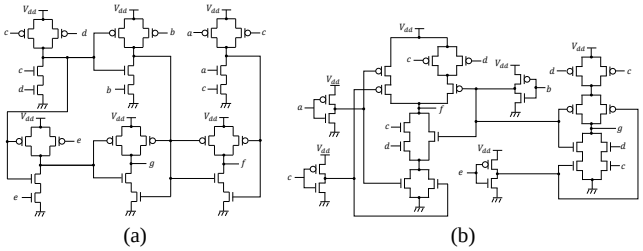
By widening the channel width of the transistor, the on-current can be increased, and the delay time can be reduced. However, an increase in channel width leads to an increase in leakage current. By selectively widening the channel width of the transistor that causes the maximum delay time in CoreGate, we aim to reduce the maximum delay time without significantly increasing leakage current.

IV. Experimental Results

A. Conditions

The experimented circuits were C17, cm82a, cm42a, cm85a, and x2 in the benchmark LGSynth91 [8]. The original circuits for cm82a and cm42a were the circuit implementations shown in [9]. For other circuits, a CMOS implementation was manually derived based on the circuit description shown in [8] and used as the original circuit.

The target LSI process was CMOS 65 nm SOTB. Using the circuit simulator HSPICE, leakage current was determined by direct current (DC) analysis, and propagation delay time from input to output was determined by transient analysis. The power supply voltages were $V_{DD} = 0.7$ V and $V_{SS} = 0$, the PMOS and NMOS substrate voltages were V_{DD} and V_{SS}, respectively. The transistor channel length was $L_P = L_N = 60$ nm for both PMOS and NMOS, and the standard channel width was $W_P = 450$ nm for PMOS and $W_N = 260$ nm for NMOS.



(a) (b)

Fig. 7. The circuit C17. (a) original. (b) converted.

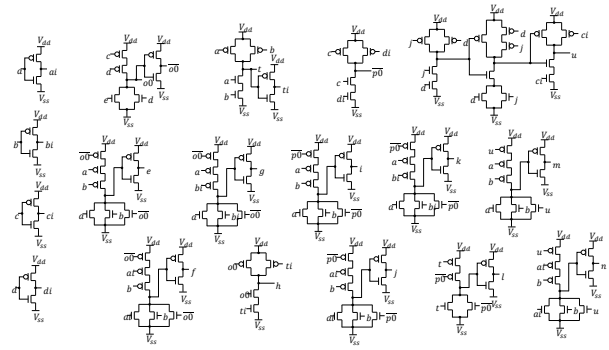


Fig. 8. The original circuit cm42a.

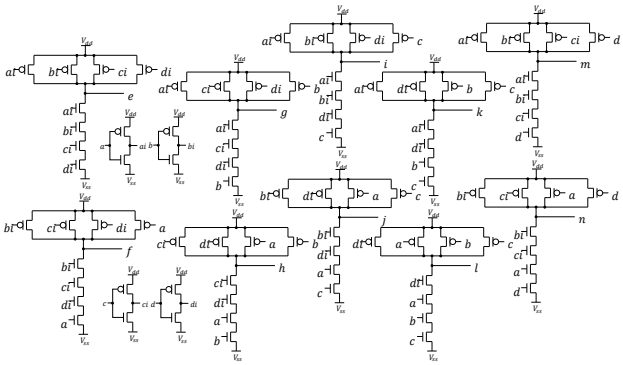


Fig. 9. The converted circuit cm42a.

The propagation delay times were determined for all combinations of input patterns that output 0 and input patterns that output 1, and the maximum, minimum, and average values were determined. In the case of a circuit having multiple outputs, the maximum and minimum values of the delay time were respectively the maximum and minimum values of all outputs, and the average value was derived by averaging the average values of each output.

B. Conversion to CoreGate structure

The original circuit and the converted circuit are shown in Fig. 7 to 15. Table I shows for each circuit the name, the number of inputs (#in), the number of outputs (#out), the number of leakage current paths (P) and the number of transistors (T) in the original and converted circuits. P_{inv} indicates the number of input inverters in the converted circuit, that is, the number of leakage current paths due to input inverters, and is included in P. It can be seen that the number of leakage current paths P is reduced by the proposed circuit conversion for all circuits

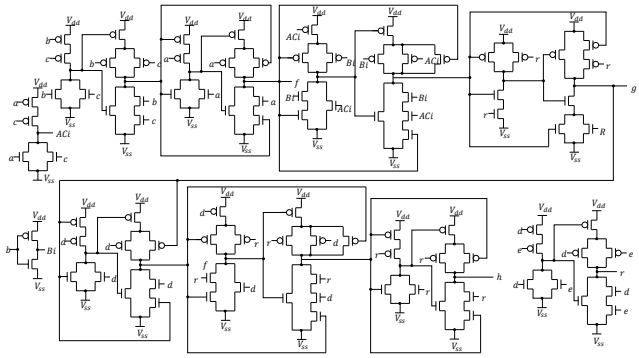


Fig. 10. The original circuit cm82a.

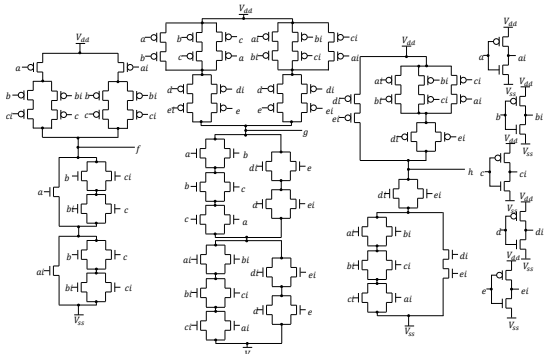


Fig. 11. The converted circuit cm82a.

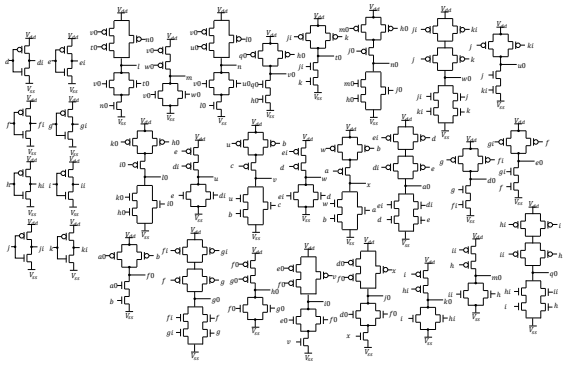


Fig. 12. The original circuit cm85a.

except circuit C17. A comparison of leakage current for each input pattern of circuit x2 is shown in Fig. 16. The leakage current of the converted circuit is reduced compared to the original circuit. A comparison of the maximum, minimum, and average values of leakage current and delay time is shown in Figs. 17 and 18. 'Orig' shows the result of the original circuit, and '1L' shows the result of the converted circuit using normal input inverters. It is confirmed from Fig. 17 that leakage current was reduced for all the circuits by the proposed circuit conversion.

C. Reduction of leakage current of input inverters

When using normal input inverters, the breakdown of the leakage current of the CoreGates and input inverters for cm42a and cm82a is shown in Fig. 19. It can be seen that depending on the input pattern, the leakage current of input inverters

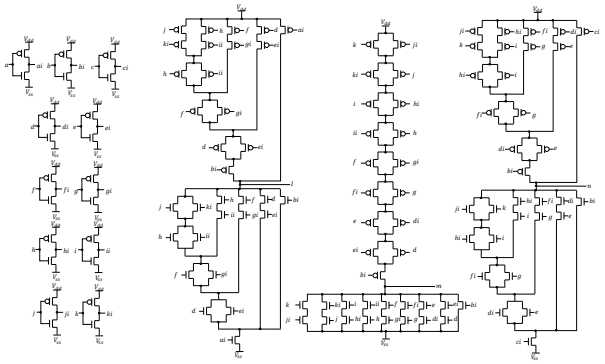


Fig. 13. The converted circuit cm85a.

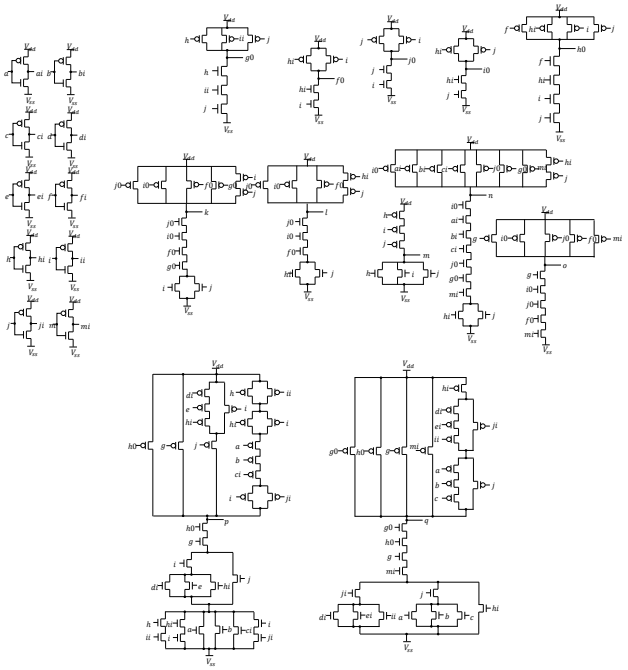


Fig. 14. The original circuit x2.

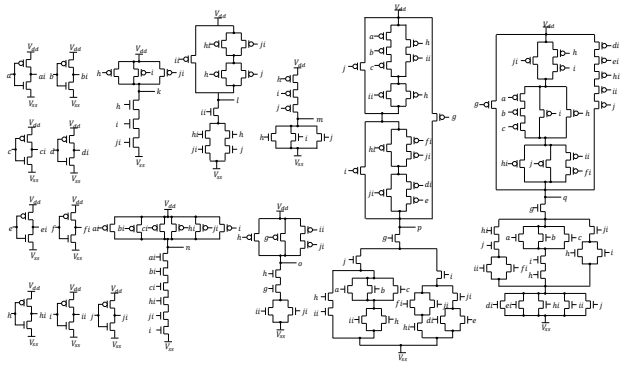


Fig. 15. The converted circuit x2.

occupies a large proportion of the total leakage current. The maximum, minimum, and average of leakage current and delay time when using a two-stage stacked input inverters are shown in Figs. 17 and 18. In these figures, '2L' represents the result of a converted circuit using the stacked input inverters.

TABLE I
COMPARISON OF LEAKAGE PATH AND TRANSISTOR COUNTS

Name	#in	#out	Original		Converted			
			P	T	P	P_{inv}	T	$T2$
C17	5	2	6	24	6	3	30	38
cm42a	4	10	31	112	14	4	88	96
cm82a	5	3	18	94	8	5	90	100
cm85a	11	3	32	144	14	11	120	142
x2	10	7	22	160	16	9	118	136

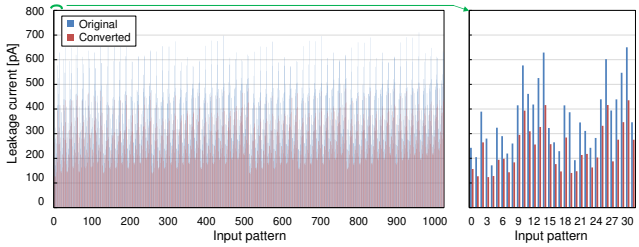


Fig. 16. The leakage current of the converted circuit x2.

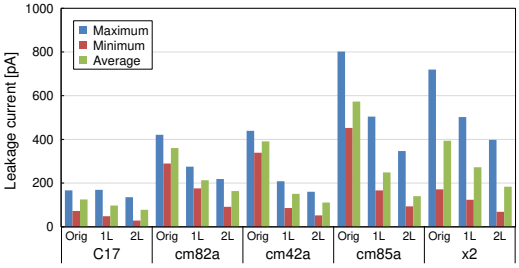


Fig. 17. The leakage current.

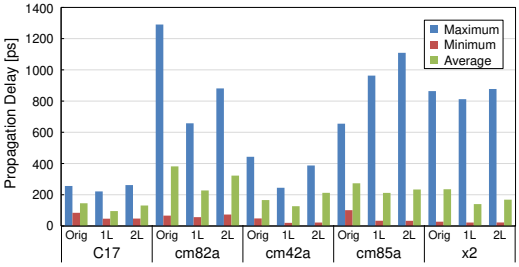


Fig. 18. The propagation delay of the original, the converted with normal inverters, and the converted with stacked inverters.

Leakage current is lowest when using the stacked input inverters. In particular, for C17, the leakage current is reduced even though the number of leakage current paths P does not decrease in the converted circuit. This is thought to be due to the effect of the transistor stack in CoreGate. On the other hand, the delay time increases when stacked input inverters are used compared to when normal input inverters are used. However, it can be seen that for cm82a and cm42a, the delay time is reduced compared to the original circuit.

The number of transistors when using two-stage stacked input inverters is shown in column $T2$ of Table I.

D. Construction of PMOS and NMOS parts

Fig. 20 shows the simulation results of leakage current and delay time for each combination of transistor connections in-

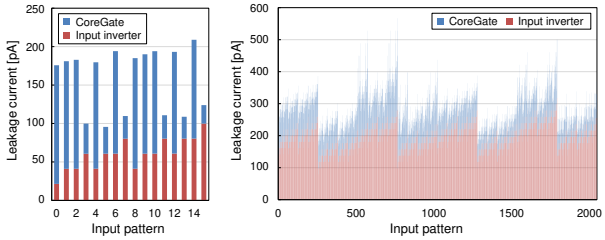


Fig. 19. Breakdown of leakage current using normal input inverters. (a) cm42a. (b) cm82a.

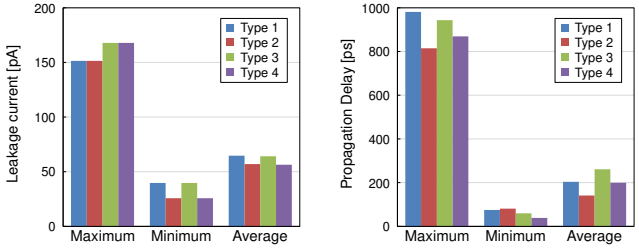


Fig. 20. The comparison of the circuit structures for the output l of cm85a.

side the PMOS part and NMOS part in the CoreGate of the output l of the circuit cm85a. There were four circuit configurations, Type 1 to Type 4, shown in Fig. 6. Among the four types, leakage current and maximum delay time of Type 2 are the lowest, and it would be explained as follows. When the output falls from a logic value 1 to a logic value 0, the NMOS part becomes conductive, thereby discharging the parasitic capacitance of the output signal wire and the drain and source of the conductive PMOS transistors. When the parallelism of the transistor connections on the output side is low, as in Type 2, more PMOS transistors are isolated from the NMOS part by shutting off PMOS transistors, resulting in less parasitic capacitance need to be discharged. As a result, the time required for the output to fall is shortened. When the output rises from a logic value 0 to a logic value 1, NMOS and PMOS are swapped, but the same can apply. Therefore, the maximum delay time of Type 2 is the smallest among 4 types, since the parallelism of transistor connections is low on the output side in both PMOS and NMOS parts in Type 2.

Similarly, for the output g of circuit cm82a with the circuit configuration shown in Fig. 21, simulation results are shown in Fig. 22. For the NMOS part, there is no noticeable difference in the parallelism of transistor connections between the side close to the output g and the side close to V_{SS}, but for the PMOS part, there is a difference in the degree of parallelism of transistor connections between the side closer to V_{DD} and the side closer to the output g. Therefore, Type 2, which has a low parallelism of transistor connections on the output side of the PMOS part, resulted in the smallest maximum delay time.

The leakage current differs slightly depending on the circuit configuration as shown in Figs. 20 and 22. This is because the voltage distribution in the source and drain of the transistors changes although there is no change in the number of leakage current paths or the number of series-connected transistors.

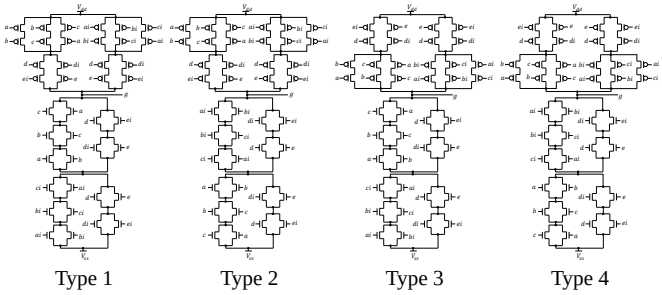


Fig. 21. Combinations of the PMOS and NMOS structures for the output *g* of cm82a.

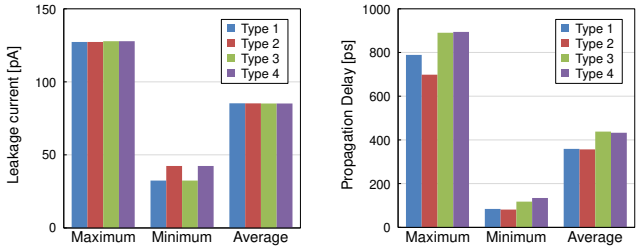


Fig. 22. The comparison of the circuit structures for the output *g* of cm82a.

E. Transistor sizing to reduce delay

The effect of reducing the delay time by changing the transistor channel width was investigated using the output *l* of circuit cm85a. For the PMOS part and NMOS part, Type 2 circuit configuration in Fig. 6 was used. To easily demonstrate the effect of changing the channel width, only the channel width of the NMOS transistors shown in Fig. 23 were changed. These transistors are on the on-current path where the delay time is at or near the maximum, and it is expected that the maximum delay time is reduced by widening the channel width. The channel width of the transistor on the output side is widened in Fig.23(a), and the channel width of the transistor on the power supply (V_{SS}) side is widened in Fig.23(b). The channel width of the transistors marked A was widened to $W_N = 310$ nm, and the transistors marked B to $W_N = 390$ nm. The results of changes in leakage current and delay time are shown in Fig. 24. Both configurations in Figs.23(a) and (b) reduce the maximum delay time, and the effect of reducing maximum delay time was larger for the configuration in Fig.23(b).

V. Conclusions

We proposed a method to reduce the static power consumption of LSI by reducing the number of leakage current paths through circuit equivalent conversion. While leakage current is reduced by using stacked input inverters, the maximum delay time tends to increase from the original circuit. The proposed method is considered effective in situations where there is delay time margin and the reduction of static power consumption is strongly needed.

Future tasks include automating layout generation, developing systematic methods for selecting transistors to widen the channel width to reduce maximum delay time, and investigating circuit conversion to reduce the number of input inverters.

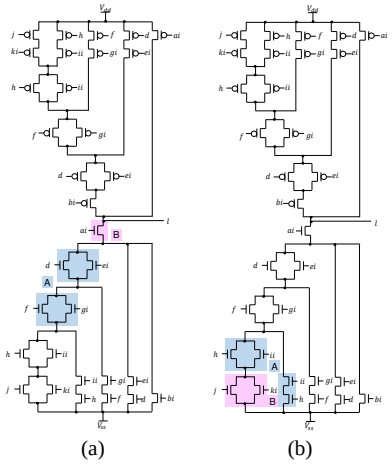


Fig. 23. Widening channel width of transistors in NMOS part for the output *l* of cm85a. (a) in the output side. (b) in the power supply side.

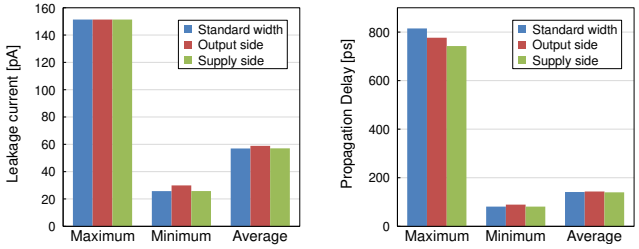


Fig. 24. The results of widening the width of transistors for cm85a.

Acknowledgements

This work was supported through the activities of VDEC, The University of Tokyo, in collaboration with NIHON SYNOPSYS G.K.

References

[1] R. Puri, L. Stok, and S. Bhattacharya, “Keeping hot chips cool,” Proceedings of the 42nd Annual Design Automation Conference, DAC ’05, New York, NY, USA, pp.285–288, Association for Computing Machinery, 2005.

[2] A.K.M.M. Islam, S. Nishizawa, Y. Matsui, and Y. Ichida, “Drive-strength selection for synthesis of leakage-dominant circuits,” 20th International Symposium on Quality Electronic Design (ISQED), pp.298–303, 2019.

[3] M.C. Johnson, D. Somasekhar, and K. Roy, “Leakage control with efficient use of transistor stacks in single threshold CMOS,” Proceedings of the 36th annual ACM/IEEE Design Automation Conference, pp.442–445, 1999.

[4] W. Lim, I. Lee, D. Sylvester, and D. Blaauw, “Batteryless sub-nW Cortex-M0+ processor with dynamic leakage-suppression logic,” 2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers, pp.1–3, 2015.

[5] N. Hanchate and N. Ranganathan, “LECTOR: a technique for leakage reduction in CMOS circuits,” IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol.12, no.2, pp.196–205, 2004.

[6] P. Gupta, A.B. Kahng, P. Sharma, and D. Sylvester, “Gate-length biasing for runtime-leakage control,” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol.25, no.8, pp.1475–1485, 2006.

[7] W. Hung, Y. Xie, N. Vijaykrishnan, M. Kandemir, M. Irwin, and Y. Tsai, “Total power optimization through simultaneously multiple-v_{DD} multiple-v_{TH} assignment and device sizing with stack forcing,” Proc. ISLPED, pp.144–149, 2004.

[8] S. Yang, “Logic synthesis and optimization benchmarks user guide: Version 3.0,” tech. rep., MCNC Technical Report, Jan. 1991.

[9] M. Garvie and P. Husbands, “Automatic synthesis of totally self-checking circuits,” ArXiv, vol.abs/1901.07023, 2019.