# CODEC system using EG2C chips and power control with a sleep mode for a visual prosthesis

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**Visual prostheses are expected to become a method of restoring sight for the blind by stimulating the visual pathway, and need further development for users. Specifically, visual prostheses require wirelessly transmitting data to implantable devices and processing the data with high speed and low power consumption. Thus, we design the dedicated CODEC chip EG2C to meet the two specifications and implement the CODEC system using EG2C chips and wireless transmission chips with a sleep mode. This paper describes the CODEC system and a method of reducing the power consumption with a sleep mode, shows the performance of the CODEC system, and proposes the CODEC system as a module of a visual prosthesis. Experimental results show EG2C chips enable to decrease the power consumption of the CODEC system by 7.56 mW.**

## I. Introduction

The population of the blind in the world is increasing and is expected to continue increasing because of population growth and population aging[1]. This suggests that the interest in restoring sight is increasing. Visual prostheses are proposed as a solution to this problem[2] and use the phenomenon called phosphene that is caused by electronically stimulating the visual cortex with electrodes[3]. Visual prostheses can be roughly categorized into visual cortical prostheses, optic nerve prostheses, and retinal prostheses[4]. Visual cortical prostheses are an attractive option due to their ability to deal with a wide range of causes of blindness. Thus, this paper investigates a visual cortical prosthesis. Visual prostheses require wireless transmission from a system outside the body to a system inside the body to prevent users from the infection from using wired transmission. However, receiving data with wireless transmission generates more heat in the body than other modules[5]. Furthermore, visual prostheses require reducing the processing time that means the delay of sight. To meet the two specifications, we design a dedicated CODEC chip of application specific integrated circuit (ASIC) called EG2C with a 16 bit application specific instruction-set processor (ASIP) to compress stimulus data, which is generated by the retinal emulator and used to control electrodes on the visual cortex[6], and implement the evaluation CODEC system composed of EG2C chips and wireless transmission chips on dedicated evaluation modules (EVMs) of printed circuit boards (PCBs).

This paper describes EG2C chips, the wireless transmission chips in the CODEC system, and the EVMs. This paper confirms the operation of the CODEC system with stimulus data of the input data, and measures the performance of the CODEC system in power consumption and processing time. The organization of this paper is as follows. Section II describes the CODEC system, and Section III shows a method of reducing the power consumption of wireless transmission chips with predicting the sleeping time. Section IV shows the experimental methods of confirming the operation and measuring the processing time and the power consumption. Section V shows the results of experiments and estimates the power consumption of EG2C chips by reducing the memory capacity. In addition, Section V evaluates the CODEC system with the reduced memory capacity in power consumption and latency by comparison. Section VI compiles the performance of the CODEC system and shows a future plan of this study.

## II. CODEC system

### A. EG2C

EG2C chips are designed to reduce the power consumption of the entire CODEC system. Table I shows the basic features of an EG2C chip, and Figure 1 shows a block diagram of an EG2C chip. EG2C chips of ASICs have the same hardware configuration as the CODEC module implemented with FPGA[7], and the frequency of the system clock is 30 MHz. The micro processing unit (MPU) compresses stimulus data with run length encoding plus exponential golomb coding and exponential golomb coding (RLE + EGC-EGC) algorithm in which EGC-EGC is conducted on the run length of both zeros and ones[8][9]. An EG2C chips have 32 KB static random access memory (SRAM) as program memory (PM) and 32 KB SRAM as data memory (DM). An EG2C chip has three univer-

TABLE I
FEATURE OF THE EG2C CHIP.

| | |
|---|---|
| Algorithm | RLE + EGC-EGC |
| System Clock | 30 MHz |
| MPU | 16 bit ASIP |
| Memory | 32 KB SRAM ×2 |
| Communication | UART 921,600 bps ×3 |
| Peripheral | Timer ×2, Interrupt controller, GPIO |
| Chip size | 5 mm × 5 mm |
| Power system | VDD Core 1.8V<br>VDDPST I/O 3.3V |
| Process rule | CMOS 180nm |

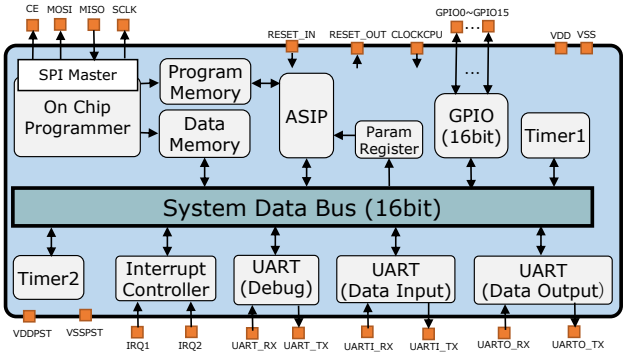


Fig. 1. EG2C Chip Block Diagram.

sal asynchronous receiver transmitters (UARTs), general-purpose input/outputs (GPIOs) and two timers. An EG2C chip, which has two kinds of power systems such as VDD Core 1.8V and VDDPST I/O 3.3V, is fabricated with CMOS 180nm technology. The chip size is 5 mm × 5 mm.

### B. *Wireless Transmission Chips*

The evaluation CODEC system uses texas instruments CC2541 system on chips (SoCs) as modules wirelessly transmitting data between the encoding side and the decoding side. In addition, the evaluation CODEC system uses CC2541 Evaluation Module Kit including two Pulse W1010 antennas and CC2541 EVMs. Table II shows the basic features of the wireless transmission chips. A CC2541 SoC has an 8051 central processing unit (CPU) that is available for general embedded systems, and wirelessly transmits data by Bluetooth low energy (BLE) 4.0. The wireless communication system in this study is GFSK 1Mbps 160 kHz deviation. The communication method between an EG2C chip and a wireless transmission chip is UART at the bit rate of 921,600 bps. CC2541 SoCs have

TABLE II
FEATURE OF THE WIRELESS TRANSMISSION CHIP[10].

| | |
|---|---|
| Core | 8051 CPU |
| Protocol | BLE 4.0 |
| Wireless Communication | GFSK 1Mbps 160 kHz deviation |
| Communication | UART, GPIO |
| Power System | VRF 3.3V |
| Current Consumption (State) | 17.9 mA (RX mode)<br>18.2 mA (TX mode)<br>1$\mu A$ (power mode 2: PM2) |


Fig. 2. EVM for the CODEC System.

the power system of VRF 3.3V and can enter power mode 2 (PM2) in which the power consumption of CC2541 SoCs is significantly lower than that in RX mode or that in TX mode. However, CC2541 SoCs in PM2 cannot communicate with other chips via UART and wireless transmission.

### C. *EVM*

The evaluation module for the CODEC system is a square PCB. Figure 2 shows the EVM on which an EG2C chip, a CC2541 SoC, a CC2541 EVM, and a Pulse W1010 antenna are attached. In Figure 2, the EG2C chip is at the center, and the CC2541 SoC, the CC2541 EVM, and the antenna are at the bottom middle. The size of the EVM is 120 mm × 120 mm.

### D. *Description of the CODEC System*

The CODEC system in this paper includes wireless transmission modules and CODEC modules to reduce the bit rate. Figure 3 shows the data flow of the CODEC system, and the following list shows the flow in detail.

1. EG2C chip for encoding receives one frame of stimulus data via UART from the stimulus data generator.
2. EG2C chip for encoding encodes the frame and transmits the encoded data to the TX SoC.
3. The encoded frame is transmitted from the TX SoC to the RX SoC at 1 Mbps.

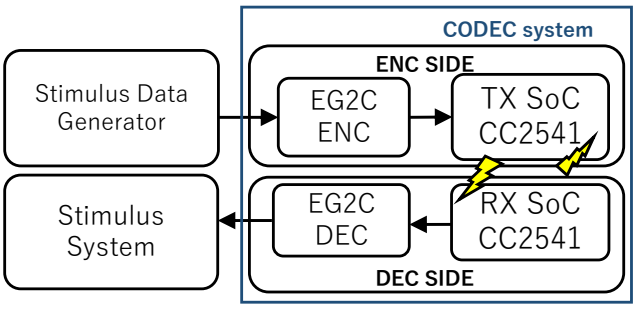


Fig. 3. Data Flow of the CODEC System.

4. EG2C chip for decoding receives the encoded frame form the RX SoC, and decodes the encoded data.

5. EG2C chip for decoding transmits the decoded frame to the stimulus system via UART.

The CODEC system processes all the 64 × 64 pixel frames of a sequence while repeating this flow at 40 fps.

## III. Power Control by Predicting the Sleeping Time

The current consumption of a CC2541 SoC for a state in Table II shows that increasing the time of staying in PM2 leads to considerably reducing the power consumption of the wirelessly transmitting (TX) SoC and that of the wirelessly receiving (RX) SoC. EG2C chips can wake up CC2541 SoCs by GPIO pulses so that CC2541 SoCs can receive stimulus data correctly. The timing of the pulse signal of a GPIO on the encoding side is decided by the encoding time and the wake-up time of PM2. In this study, the timing of the pulse signal on the encoding side is when the rest size of frame data received by the EG2C chip for encoding is 16 Bytes.

Decision of the timing of a pulse signal of a GPIO on the decoding side requires predicting the time when the TX SoC wirelessly transmit data not to miss stimulus data. The data size of a compressed frame of stimulus data tends to be as large as that of the next compressed frame. This feature enables the EG2C chip for decoding to predict the timing. If the data size of a compressed frame is equal to that of the next compressed frame and the method of the wired transmission to the EG2C chip for encoding is not changed, the sleeping time is predictable because the delay between the start of receiving a frame from the stimulus data generator and the start of wirelessly transmitting the compressed frame mainly depends on the data size of the compressed frame.

Table III shows the predicting sleeping time of the RX SoC for the data size of a compressed frame. Table III is made by following the method.

TABLE III
Predicting Sleeping Time of the TX SoC.

| Data size [Bytes] | Time [ms] | Data size [Bytes] | Time [ms] |
|---|---|---|---|
| [0000, 000C) | 21.85 | [0078, 0080) | 12 |
| [000C, 0017) | 21 | [0080, 008D) | 11 |
| [0017, 0025) | 20 | [008D, 0095) | 10 |
| [0025, 0031) | 19 | [0095, 00A0) | 9 |
| [0031, 003B) | 18 | [00A0, 00A9) | 8 |
| [003B, 0048) | 17 | [00A9, 00B5) | 7 |
| [0048, 0054) | 16 | [00B5, 00C4) | 6 |
| [0054, 0062) | 15 | [00C4, 00D3) | 5 |
| [0062, 006F) | 14 | [00D3, 00E2) | 4 |
| [006F, 0078) | 13 | [00E2, FFFF] | 0 |

1. Measure the duration between the time when the EG2C chip for decoding finishes receiving a frame and the time when the EG2C chip for encoding starts transmitting the next frame for a data size.

2. Round the time down and reduce the minimum unit of the time to 1 ms.

3. Find a section in which the fixed time for a data size is equal to that for a different data size.

4. Make the look-up table (LUT) by compiling the sections.

The EG2C chip for decoding has the LUT of Table III in Data Memory, and compares the data size sections with the data size of the compressed frame when finishing receiving a compressed frame and decides the sleeping time of the TX SoC. As an example of predicting the sleep time, when the data size of a compressed frame is 16'h 0031 Bytes, the RX SoC sleeps for 18 ms after transmitting to the EG2C chip for decoding. The average data size of compressed frames of stimulus data is 16'h 0081 Bytes.

## IV. Experiment

### A. Experimental setup of the CODEC System

This experiment aims to confirm the operation of the CODEC system using EG2C chips and CC2541 SoCs by comparing stimulus data input to the encoding module with stimulus data output from the decoding module and confirming that input stimulus data is consistent with output stimulus data in 11 scenes. Figure 4 shows an operation confirmation environment. The TX controller of dedicated circuits, which can transmit the designated number of frames of stimulus data of 64 × 64 pixels at 40 fps, is designed to transmit stimulus data to the EG2C chip for encoding via UART. All the frames for a sequence

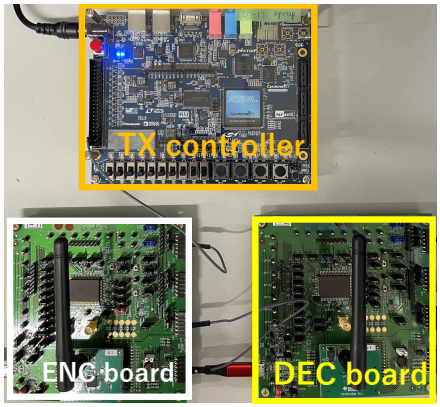


Fig. 4. Operation Confirmation Environment.The FPGA at the top center is the TX controller. The EVM at the bottom left is the ENC board. The EVM at the bottom right is the DEC board.

are transmitted by the TX controller as input stimulus data, and all the frames for a sequence are transmitted by the EG2C chip on the DEC board side as output stimulus data. The distance between the antenna on the TX SoC and that on the RX SoC is set to 20 cm.

### B. *Measurement of the Processing Time*

This experiment aims to measure the total processing time of the CODEC system for a frame with GPIO pulse signals of EG2C chips. The total processing time of the CODEC system indicates the partial latency of a visual prosthesis to gain sight excluding the latency of generating stimulus data and that of stimulating the brain with an electrode array.

### C. *Measurement of the Power Consumption*

This experiment aims to measure the power consumption of chips in the CODEC system such as EG2C chips, the TX SoC, and the RX SoC in Figure 3. Because heat generated by devices in the body of a user leads to increasing the temperature of organ surrounding the devices, the power consumption is an important factor in designing a visual prosthesis. Current sense shunt resistors and input voltages are connected in series, and the voltage drop across the resistor is measured. Table IV shows a list of input voltages of chips in the CODEC system and shunt resistors connected with the input voltages. The power consumption is calculated with the voltage across the resistor, the resistance of the resistor, and the input voltage of the chip dropped by the resistor.

TABLE IV
Current Sense Shunt Resistors.

| ENC/DEC | Power system | Input voltage[V] | Resistance[Ω] |
|---|---|---|---|
| ENC | VDD Core | 1.8 | 66.57 |
| | VDDPST I/O | 3.3 | 992.3 |
| | VRF | 3.3 | 21.89 |
| DEC | VDD Core | 1.8 | 66.52 |
| | VDDPST I/O | 3.3 | 992.3 |
| | VRF | 3.3 | 21.87 |

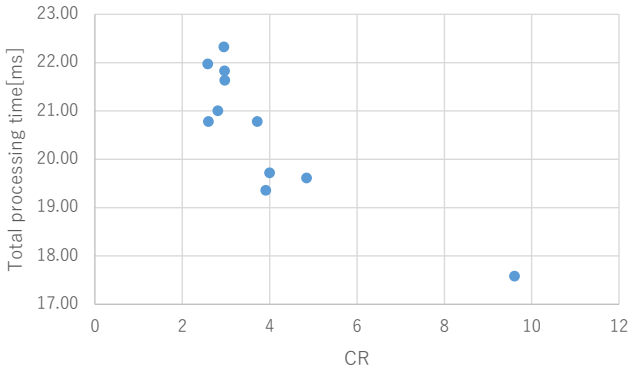


Fig. 5. Relation between the CR and the Total Processing Time.

## V. Evaluation and Discussions

### A. *Result of the Operation Confirmation*

The output data of the CODEC system are completely restored in all the test scenes. Thus, the CODEC system with the sleep control processes 64 × 64 pixel stimulus data at 40 fps works correctly.

### B. *Processing Time of the CODEC System*

Table V shows the result of measuring the processing time of a frame of the CODEC system for a scene. This result shows the total processing time for a scene widely ranges from 17.59 ms to 22.33 ms. Figure 5 shows a scatter plot of the compression ratio (CR) and the total processing time for a scene. The CR for a scene is calculated by the total data size of raw stimulus data for a scene divided by the total data size of compressed stimulus data for a scene. High CRs mean efficiently compressed data. The correlation coefficient between the CR and the total processing time is -0.86. Thus, this result indicates increase of CRs by compression leads to reducing the total latency of the CODEC system.

### C. *Power Consumption of the CODEC System*

Table VI shows the result of measuring the total power consumption of both the two chips on the ENC board

TABLE V
PROCESSING TIME OF THE CODEC SYSTEM.

| Scene No. | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | Ave. [ms] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Processing time | 20.78 | 19.72 | 19.36 | 21.01 | 21.64 | 20.78 | 22.33 | 17.59 | 21.83 | 19.62 | 21.97 | 20.67 |

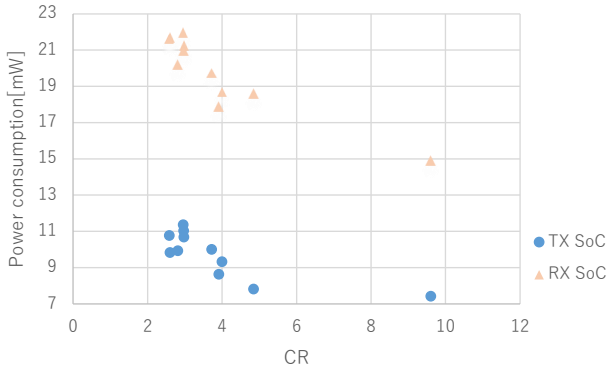


Fig. 6. Relation between the CR and the Power Consumption.

and that on the DEC board in the CODEC system for a scene with the current sense shunt resistors in Table IV. In addition, Table VI shows the result of measuring the total power consumption of the CODEC system for a scene without the power control. The TOTAL power consumption contains the power consumption of all the power system including EG2C and VRF.

The power consumption of the EG2C for encoding ranges from 10.58 mW to 10.71 mW, and that for decoding ranges from 10.91 mW to 11.12 mW. Thus, this result indicates that the power consumption of EG2C chips is steady in all the scene regardless of CRs. Figure 6 shows a scatter plot of the CR and the power consumption of the TX and RX SoC for a scene. The correlation coefficient between the CR and the power consumption in the TX SoC is -0.78, and that in the RX SoC is -0.90. Thus, these two results indicates increase of CRs by compression leads to reducing the power consumption of the RX SoC and the TX SoC as well.

Comparing the power consumption in the CODEC system with that in the CODEC system without the sleep control, the average power consumption of the TX SoC for a scene in the CODEC system is 14.12 mW lower than that in the CODEC system without the power control. The average power consumption of the RX SoC for a scene in the CODEC system is 47.23 mW lower than that in the CODEC system without the power control. Therefore, these results show that the power control using predicting the sleeping time reduces the power consumption of the CODEC system significantly.

### D. *Improvement in Power Consumption*

An EG2C chip has 32 KB Program Memory and 32 KB Data Memory, whose capacities are designed largely comparing to the program and data size used in the current CODEC system. The unused memory area is room for the scalability for future applications. According to the logic synthesis report, the dynamic power consumption of PM and DM occupies 71.5% of the total power consumption of an EG2C chip. The two EG2C chips use up to 2 KB in PM and up to 2 KB in DM to implement the current CODEC system. Table VII shows the result of estimation of the power consumption of 4 KB SRAM. The measured power consumption of 64 KB SRAM minus the estimated power consumption of 4 KB SRAM is 5.11 mW. This calculated result shows reduction of the memory capacities enables further reduction of the power consumption of an EG2C chip by 5.11 mW.

### E. *Comparing Systems including the CODEC System*

Table VIII shows the performance of the CODEC system improved by reducing the memory capacities and that of the wireless transmission system without EG2C chips. Comparing the improved CODEC system and the wireless transmission system, the TOTAL power consumption of the improved CODEC system is 7.56 mW lower than that of the wireless transmission system, and the latency of the CODEC system is 3.09 ms longer than that of the wireless transmission system.

## VI. CONCLUSIONS

This study describes the CODEC system that processes stimulus data of 64 × 64 pixels at 40 fps, and confirms the operation and reducing the power consumption by the sleep control predicting the available sleeping time. Through measuring the power consumption, we demonstrate that EG2C chips enable reduction of the power consumption by 7.56 mW. In addition, we show strong negative correlations between the CR and the performance. This means that finding high compression ratio algorithms is effective to improve the performance of the CODEC system further when using the wireless transmission chips.

We have a future plan with the CODEC system. The plan is to implement the CODEC system in an environment that emulate human organs and measure increase of the temperature by operation of the CODEC system.

TABLE VI
Power Consumption of the CODEC System.

| Scene No. | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | Ave. [mW] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CODEC system with power control | ENC | EG2C | 10.62 | 10.67 | 10.58 | 10.61 | 10.67 | 10.63 | 10.71 | 10.60 | 10.64 | 10.63 | 10.61 | 10.63 |
| | | VRF | 9.83 | 9.32 | 8.63 | 9.93 | 10.68 | 10.00 | 11.36 | 7.41 | 11.03 | 7.81 | 10.77 | 9.71 |
| | | TOTAL | 20.45 | 19.99 | 19.21 | 20.54 | 21.35 | 20.63 | 22.07 | 18.01 | 21.67 | 18.44 | 21.38 | 20.34 |
| | DEC | EG2C | 11.09 | 11.00 | 11.01 | 11.09 | 11.07 | 11.04 | 11.12 | 10.91 | 11.09 | 11.00 | 11.11 | 11.05 |
| | | VRF | 21.70 | 18.67 | 17.87 | 20.19 | 21.25 | 19.72 | 21.96 | 14.89 | 20.96 | 18.61 | 21.60 | 19.77 |
| | | TOTAL | 32.79 | 29.67 | 28.88 | 31.28 | 32.32 | 30.75 | 33.08 | 25.80 | 32.05 | 29.61 | 32.71 | 30.81 |
| Without power control | ENC | VRF | 23.60 | 23.56 | 23.35 | 23.98 | 24.26 | 23.85 | 24.61 | 22.68 | 24.33 | 23.49 | 24.38 | 23.83 |
| | | TOTAL | 34.33 | 34.46 | 34.15 | 34.81 | 35.15 | 34.61 | 35.64 | 33.55 | 35.25 | 34.41 | 35.23 | 34.69 |
| | DEC | VRF | 67.01 | 67.53 | 67.17 | 66.89 | 66.73 | 67.06 | 65.62 | 68.65 | 66.47 | 67.54 | 66.25 | 66.99 |
| | | TOTAL | 78.92 | 79.39 | 79.17 | 78.81 | 78.66 | 78.96 | 77.62 | 80.54 | 78.43 | 79.42 | 78.17 | 78.92 |
| VRF diff. | ENC | | | | | | - | | | | | | | 14.12 |
| | DEC | | | | | | - | | | | | | | 47.23 |

TABLE VII
Estimation of the Power Consumption of SRAM.

| Capacity [KB] | Catalog [mW] | Power consumption[mW] | Ratio |
|---|---|---|---|
| 64 (32 + 32) | 12.52 | 8.098 (Measured) | 0.6468 |
| 4 (2 + 2) | 4.620 | 2.988 (4.620 × 0.6468) | |
| Difference | | -5.11 | |

TABLE VIII
Evaluation of the Performance.

| System | Power Consumption [mW] | | | Latency[ms] |
|---|---|---|---|---|
| | ENC | DEC | TOTAL | |
| CODEC with 4KB SRAM | 15.23 | 25.70 | 40.93 | 20.67 |
| Wireless transmission | 20.77 | 27.72 | 48.49 | 17.58 |
| Difference | -5.54 | -2.02 | -7.56 | +3.09 |

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