A Comparator with Controllable Offset Voltage Variation for Stochastic Flash ADC

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Abstract— We propose a comparator with controllable offset voltage variation for stochastic flash ADC. The proposed comparator is based on a conventional StrongARM comparator, and additional transistors control the differential pair's currents to control the offset voltage variation. The circuit simulation results show that the standard deviation of the offset voltages variation is changed from 17.4 mV to 74.7 mV by digital control when a reference voltage V_{ref} is 0.9 V.

I. Introduction

As CMOS processes are scaled to smaller technology nodes, the performance of LSIs has improved. However, the performance of analog LSIs has degraded due to the variation of MOSFET's threshold voltage [1]. An analog-to-digital converter (ADC) becomes especially inaccurate because the offset voltage of the comparator depends on the variation. For example, in the case of a flash ADC, a resistor ladder or a similar circuit is used to generate comparators' trip points corresponding to each digital code. As the resolution of the flash ADC increases, the 1 LSB becomes smaller, and the constraints of reference voltage fluctuations and the comparator offset voltage variations become more severe. Various calibration methods have been studied to solve them. As a candidate for overcoming it, a stochastic flash ADC was proposed [2]. A stochastic flash ADC uses variations in the input offset voltage of a comparator as the trip points. Since the input offset voltage distribution is the probability density function (PDF) similar to the Gaussian distribution, the transfer function of the stochastic flash ADC is the cumulative distribution function (CDF) of the offset voltages. The input voltage range of the stochastic flash ADC is narrow because it is from $-\sigma$ to $+\sigma$, where the CDF is close to the linear characteristics.

A swapping method of CDF was proposed to extend the input voltage range of the stochastic flash ADC [3]. However, this method needs more comparators, and kickback noise affects the input voltage range depending on increased comparators. As another approach, a flash ADC architecture that selects the minimum number of comparators based on order statistics was proposed to solve the kickback noise issue and improve the linearity of the transfer function [4]. However, available ADC's resolution decreases, and the input voltage range of [4] is narrow because the offset voltage variation of comparators used in stochastic flash ADC is almost the same as the previous ones.

Thus, stochastic flash ADC requires extending the input voltage range and externally calibrating the offset voltage distribution of the comparator. In this study, we propose a comparator with controllable offset voltage variation for stochastic flash ADC that exploits offset voltage variation such as.

II. StrongARM comparator's offset voltage

In this study, we use the StrongARM comparator shown in Fig. 1 [5]. V_A and $V_{A'}$ of the strongARM comparator are precharged to V_{DD} if CLK is V_{SS}, where V_A and $V_{A'}$ are the voltages of node A and A$'$, respectively. V_A and $V_{A'}$ of StrongARM comparator go down when CLK rises from V_{SS} to V_{DD}. If input voltage V_{in} is higher than reference voltage V_{ref}, I_{Mn1} is also larger than I_{Mn2}. I_{Mn1} and I_{Mn2} are the currents that flow from A and A$'$ to V_{SS} through M_{n1} and M_{n2}, respectively. Thus, V_A reaches $V_{DD}-|V_{thp}|$ (V_{thp} is the threshold voltage of PMOS) earlier than $V_{A'}$ in Fig. 2. As a result, the output of the StrongARM comparator is decided according to V_A goes V_{SS} and $V_{A'}$ recharges V_{DD}. t_0 is the time when V_A and $V_{A'}$ start to go down from V_{DD}, t_1 and t_2 are the time when V_A and $V_{A'}$ reach $V_{DD}-|V_{thp}|$ in Fig. 2. If V_{in} is equal to V_{ref} and no MOSFET variation exists, t_1 is equal to t_2 because I_{Mn1} and I_{Mn2} are the same. If MOS-

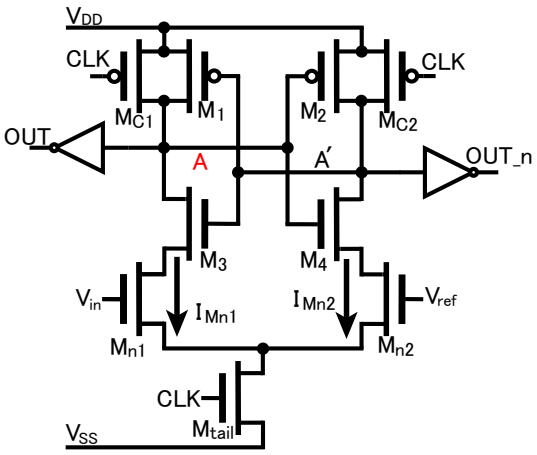

Fig. 1. StrongARM comparator.

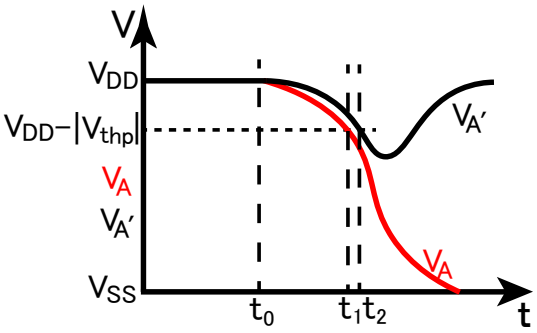

Fig. 2. Operation phases for the StrongARM comparator.

FET has threshold voltage variation, t_1 is not equal to t_2 because of the current mismatch between I_{Mn1} and I_{Mn2} even when V_{in} is equal to V_{ref}. For example, if M_{n1}'s threshold voltage V_{thnMn1} is larger than M_{n2}'s threshold voltage V_{thnMn2}, $t_1 > t_2$ because I_{Mn1} is smaller than I_{Mn2} even when V_{in} and V_{ref} are the same. If the variation of V_{thnMn1} and V_{thnMn2} exists, input offset voltage V_{OS1} is the voltage that satisfies $V_{in} + V_{OS1} = V_{ref}$.

M_{n1} and M_{n2} work in saturation region until t_1 or t_2. The drain currents I_{Mn1} and I_{Mn2} are expressed as

$$I_{Mn1} = \frac{\beta_{n1}}{2}(V_{in} - V_{thn} - \Delta V_{thnMn1})^2 \quad (1)$$

$$I_{Mn2} = \frac{\beta_{n2}}{2}(V_{ref} - V_{thn} - \Delta V_{thnMn2})^2 \quad (2)$$

where ΔV_{thnMn1} and ΔV_{thnMn2} are the variation in threshold voltages of M_{n1} and M_{n2}, respectively. Also, β is the current amplification factor of MOSFET, and V_{thn} is the threshold voltage of NMOS without variations. V_{in} and V_{ref} can be written as a function of the current and

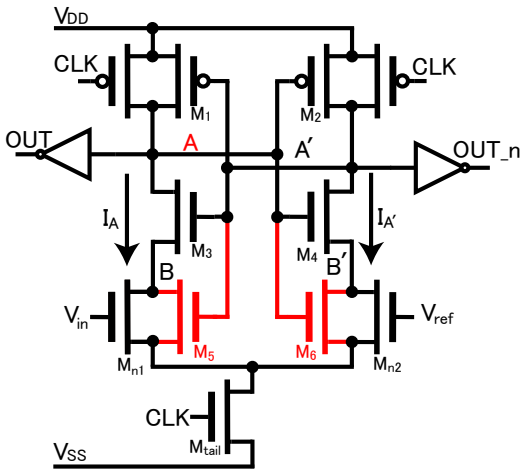

Fig. 3. StrongARM comparator with expanded the offset voltage variation.

threshold voltage based on (1) and (2) as follows:

$$V_{in} = \sqrt{\frac{2I_{Mn1}}{\beta_{n1}}} + V_{thn} + \Delta V_{thnMn1} \quad (3)$$

$$V_{ref} = \sqrt{\frac{2I_{Mn2}}{\beta_{n2}}} + V_{thn} + \Delta V_{thnMn2} \quad (4)$$

$I_{Mn1} = I_{Mn2}$ is satisfied when $\beta_{n1} = \beta_{n2}$, $V_{in} + V_{OS1} = V_{ref}$. Thus, the offset voltage in Fig. 1 can be expressed as

$$V_{OS1} = \Delta V_{thnMn2} - \Delta V_{thnMn1}. \quad (5)$$

III. A StrongARM comparator with controllable offset voltage variation

As described in the previous section, the StrongARM comparator's offset voltage varies because of the current mismatch between I_{Mn1} and I_{Mn2} according to the threshold voltage variation. If the current variation caused by the threshold voltage variation is enlarged, the comparator's offset voltage variation will be extended. We propose the comparator in Fig. 3 to enlarge the current variation. M_5 and M_6 are added so that the currents I_A and $I_{A'}$ are more varied when V_A and $V_{A'}$ go down. I_A and $I_{A'}$ become $I_{Mn1}+I_{M5}$ and $I_{Mn2}+I_{M6}$, respectively. If the variation of V_{thnMn1}, V_{thnMn2}, V_{thnM5} and V_{thnM6} exists, input offset voltage V_{OS2} is the voltage that satisfies $V_{in}+V_{OS2} = V_{ref}$ in Fig. 3. M_5 and M_6 have the drain voltage V_B and $V_{B'}$ that are lower than V_A and $V_{A'}$ that precharged to V_{DD}. Thus, M_5 and M_6 operate in triode region. The drain currents I_{M5} and I_{M6} are expressed as

$$I_{M5} = \beta_5(V_{A'} - V_{thn} - \Delta V_{thnM5} - \frac{V_B}{2})V_B \quad (6)$$

$$I_{M6} = \beta_6(V_A - V_{thn} - \Delta V_{thnM6} - \frac{V_{B'}}{2})V_{B'} \quad (7)$$

where ΔV_{thnM5} and ΔV_{thnM6} are the threshold voltages variation of M_5 and M_6, respectively. The currents I_A and $I_{A'}$ can be written based on (1)-(7) as follows:

$$\begin{aligned} I_A &= I_{Mn1} + I_{M5} \\ &= \frac{\beta_{n1}}{2}(V_{in} - V_{thn} - \Delta V_{thnMn1})^2 \\ &+ \beta_5(V_{A'} - V_{thn} - \Delta V_{thnM5} - \frac{V_B}{2})V_B \end{aligned} \quad (8)$$

$$\begin{aligned} I_{A'} &= I_{Mn2} + I_{M6} \\ &= \frac{\beta_{n2}}{2}(V_{ref} - V_{thn} - \Delta V_{thnMn2})^2 \\ &+ \beta_6(V_A - V_{thn} - \Delta V_{thnM6} - \frac{V_{B'}}{2})V_{B'} \end{aligned} \quad (9)$$

If each current amplification factor is $\beta_{n1} = \beta_{n2} = \beta_5 = \beta_6 = \beta_n$, V_{in} and V_{ref} can be written as a function of the current and threshold voltage based on (8) and (9) as follows:

$$V_{in} = \sqrt{\frac{2I_{Mn1}+2I_{M5}}{\beta_n} - 2V_B \times \Delta V_{thnM5} + K_{in}} + V_{thn} + \Delta V_{thnMn1} \quad (10)$$

$$V_{ref} = \sqrt{\frac{2I_{Mn2}+2I_{M6}}{\beta_n} - 2V_{B'} \times \Delta V_{thnM6} + K_{ref}} + V_{thn} + \Delta V_{thnMn2} \quad (11)$$

where

$$K_{in} = -2V_B \times (V_{A'} - V_{thn} - \frac{V_B}{2}) \quad (12)$$

$$K_{ref} = -2V_{B'} \times (V_A - V_{thn} - \frac{V_{B'}}{2}). \quad (13)$$

$I_A = I_{A'}$ is satisfied when $V_{in} + V_{OS2} = V_{ref}$. Thus, the offset voltage in Fig. 3 can be expressed as

$$\begin{aligned} V_{OS2} &= \sqrt{\frac{2I_{Mn2}+2I_{M6}}{\beta_n} - 2V_{B'} \times \Delta V_{thnM6} + K_{ref}} \\ &- \sqrt{\frac{2I_{Mn1}+2I_{M5}}{\beta_n} - 2V_B \times \Delta V_{thnM5} + K_{in}} \\ &+ V_{OS1}. \end{aligned} \quad (14)$$

The offset voltage V_{OS2} is varied with the magnitude of I_A and $I_{A'}$ and the threshold voltage variations of M_5 and M_6 in addition to the conventional offset voltage V_{OS1}. As a result, the variation of V_{OS2} is larger than V_{OS1}. In addition, it is possible to control the offset voltage V_{OS2} if the magnitude of I_A, $I_{A'}$ and the variation of the M_5 and M_6 can be controlled.

In this study, we propose to control the currents of MOSFET M_5 and M_6 in order to control the offset voltage variation. The currents are controlled by adding M_7 and M_8, and switches SW_1, SW_2, as shown in Fig. 4. SW_1 and SW_2 turn on when digital signal S is high. On the other hand, if SW_1 and SW_2 turn off, the magnitudes of I_{M5} and I_{M6} are smaller than in the previous case because the currents flow through M_7 and M_8. In addition, ΔV_{thnM5} and ΔV_{thnM6} of (12) are small because the threshold voltage variations of M_5, M_6, M_7 and M_8 are averaged by connected in series. Thus, the comparator in Fig. 4 has smaller offset voltage variation when S is high and has larger one when S is low.

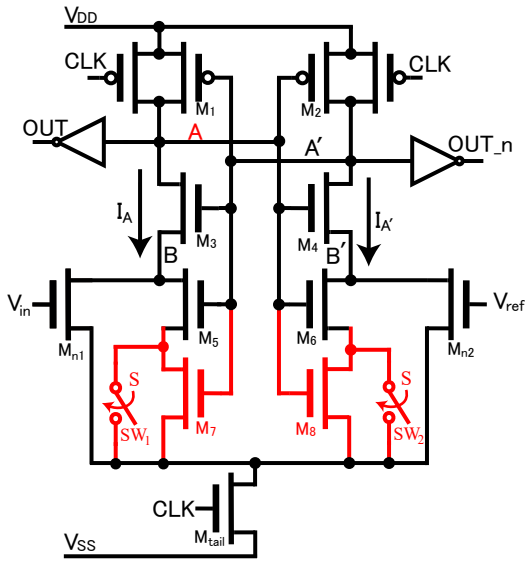

Fig. 4. A comparator with controllable offset voltage variation.

IV. Simulation results

In this study, ROHM 0.18 μm CMOS process is used, and a circuit simulation was performed using HSPICE from Synopsys. We simulated the offset voltage of the comparator a thousand times for Monte Carlo analysis considering a standard deviation of 3 mV as the MOSFET's threshold voltage. The power supply voltage V_{DD} and CLK frequency were 1.8 V and 100 MHz. We evaluated the offset voltage variation of the StrongARM comparator with extended offset voltage variation and the comparator with controllable offset voltage variation.

A. *Simulation results of StrongARM comparator with expanded offset voltage variation*

We analyzed the variation of the StrongARM comparator with an extended offset voltage variation. All gate lengths and widths of the MOSFETs are designed with minimum sizes to extend the threshold voltage variation. To obtain the offset voltage distribution of the conventional StrongARM comparator and the comparator in Fig. 3, Monte Carlo analysis was carried out with 1000

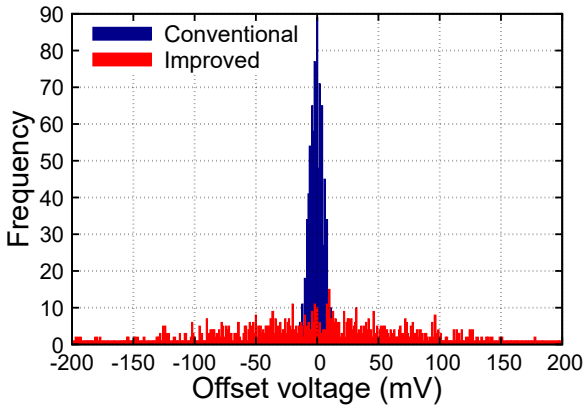

Fig. 5. The histogram plots of the offset voltage variation of the conventional StrongARM comparator and the comparator in Fig. 3.

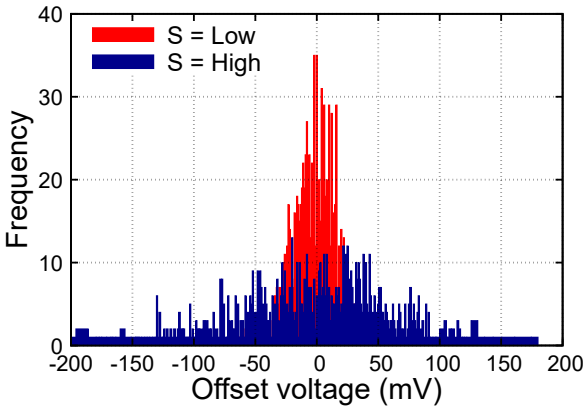

Fig. 6. The histogram plots of the offset voltage variation of the comparator with controllable offset voltage variation.

iteration runs at the reference voltage (V_{ref} = 0.9 V). Fig. 5 illustrates the histogram plots of the offset voltage and frequency for both comparators. It can be seen that the standard deviation of the offset voltage variation varied from 5.5 mV to 101.0 mV. Therefore, the comparator in Fig. 5 can increase the standard deviation of offset voltage by approximately 18.4 times compared to the conventional StrongARM comparator with almost the same sizes MOSFETs.

B. *Simulation results of the comparator with controllable offset voltage variation*

We analyzed the offset voltage variation of the comparator with controllable offset voltage variation by controlling the currents MOSFET M_5 and M_6. We assumed switches SW_1 and SW_2 in Fig. 4 to be ideal switches. To verify the distribution of the comparator with controllable offset voltage variation when digital signal S is High or Low, Monte Carlo analysis was carried out with 1000 iteration runs at the reference voltage (V_{ref} = 0.9 V). Fig. 6 illustrates the histogram plots of the offset voltage and frequency for the comparator with controllable offset voltage variation when digital signal S is High or Low. It can be seen that the standard deviation of the offset voltage variation is changed from 17.4 mV to 74.7 mV by changing S from Low to High. Therefore, the comparator in Fig. 4 can increase the standard deviation of offset voltage variation by approximately 4.3 times according to digital control.

V. Conclusion

We proposed a comparator with controllable offset voltage variation that is based on a conventional StrongARM comparator and additional transistors for controlling the offset voltage variation. The circuit simulation results show that the standard deviation of the proposed comparator can be changed from 17.4 mV to 74.7 mV by increasing the magnitudes and variation of the differential pair's currents at the reference voltage (V_{ref} = 0.9 V). The proposed comparator is effective for circuits that require external calibration and extending the comparator offset voltage variation such as stochastic flash ADC.

Acknowledgements

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